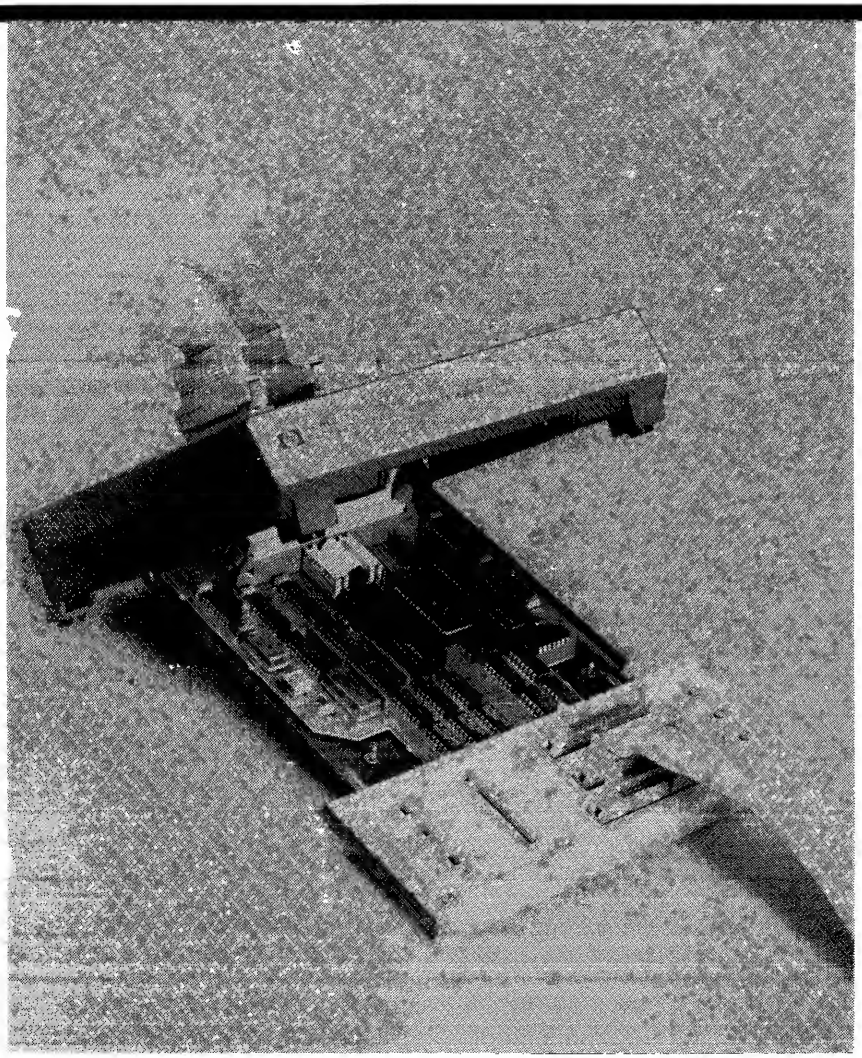
HP 10342B Bus Preprocessor

(HP 1650A/51A and HP 16510A)

Operating Manual



HEWLETT PACKARD

Bus Preprocessor Operating Manual

HP 10342B
Bus Preprocessor

for the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers

Manual Set Part Number 10342-90912
Microfiche Part Number 10342-90812

Printed in U.S.A November 1987

Printing History First Edition - November 1987 Printed in U.S.A.

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of 1 year from date of shipment. During warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. However, warranty service for products installed by Hewlett-Packard and certain other products designated by Hewlett-Packard will be performed at Buyer's facility at no charge within the Hewlett-Packard service travel area. Outside Hewlett-Packard service travel areas, warranty service will be performed at Buyer's facility only upon Hewlett-Packard's prior agreement and Buyer shall pay Hewlett-Packard's round trip travel expenses.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument, software, or firmware will be uninterrupted or error-free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Exclusive Remedies

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this operating manual.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

Safety

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this operating manual must be heeded.

Table of Contents

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Introduction

The HP 10342B Bus Preprocessor, with the HP 10269C General Purpose Probe Interface, provides an easy connection between the HP 1650A/51A or HP 16510A Logic Analyzers and three popular data buses, HP-IB (Hewlett-Packard's implementation of IEEE 488- 1978), RS-232-C/CCITT V.24, and RS-449.

The HP 10342B software provides inverse assembly of activity on the buses, and configurations for the logic analyzers. Any information in this manual about the usage of the HP 1650A/51A or HP 16510A Logic Analyzers is supplementary to that provided in the logic analyzer operation and programming manuals.

The appendices contain abbreviated versions of the standards for the buses. Additional information should be obtained from the appropriate standards organization for each bus.

The manual is organized into six chapters.

Chapter 1 covers general information such as product description and accessories.

Chapter 2 covers general hardware information, such as inspection, power requirements, maintenance, and troubleshooting.

Chapter 3 covers general information about the software supplied.

Chapter 4 covers use of the HP 10342B for preprocessing the HP-IB. It includes installation and other information specific to using the HP 10342B on this bus.

Chapter 5 covers the use of the HP 10342B for preprocessing the RS-232-C/CCITT V.24 bus. It includes installation and other information specific to using the HP 10342B on this bus.

Chapter 6 covers use of the HP 10342B for preprocessing the RS-449 bus. It includes installation and other information specific to using the HP 10342B on this bus.

The appendices provide some of the basic specifications of the three buses handled by the HP 10342B.

1 General Information

Introduction

The HP 10342B Bus Preprocessor combines in one instrument the capability for analyzing three popular buses. The HP 10342B consists of an interface module which plugs into the HP 10269C General Purpose Probe Interface. Three connectors on the front panel of the interface module accept cables which connect with the bus being tested. Switches on the front panel are set up to match the parameters of the signals on the bus.

The inverse assembler and configuration files loaded into the logic analyzer from the disc set up the basic analysis parameters. The operator can further set up the analyzer to make and process the measurements in other ways. The exact measurement capabilities depend on the logic analyzer being used.

HP-IB

The HP-IB input to the HP 10342B provides one HP-IB defined load to the bus being monitored. The data and handshake lines of the bus are buffered and run directly to the probe connectors of the HP 10269C.

RS-232-C/CCITT V.24

The RS-232-C input to the HP 10342B provides one RS-232-C defined load on the bus being monitored. The lines of the bus under test are buffered and applied to circuitry that takes the serial data stream and converts it back into original data and status. The HP 10342B monitors five handshake lines and their status is stored with each character received. Four switches set up the protocol and data rates. A microprocessor controls the functions in the preprocessor.

RS-449

The RS-449 input to the HP 10342B provides one RS-449 defined load on the bus being monitored. The lines of the bus are buffered and ORed with the buffered lines from the RS-232-C connector. From that point, RS-449 uses the same circuitry to capture the serial data as used by RS-232-C. RS-449 inverse assembler and configuration files are provided for the logic analyzer.

Operating Characteristics

Table 1-1 gives operating characteristics of the HP 10342B.

Table 1-1. HP 10342B Specifications and Operating Characteristics

RS-232C and RS-449*	
Asynchronous Data	
Data Transfer Rates (bits/second)	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200
Bits per Character	6, 7, or 8
Data Format	6-bit transcode, 7 or 8-bit ASCII, 8-bit EBCDIC Odd, even, or no parity 1, 1.5, or 2 stop bits

* Note: The HP 10342B supports both RS-422A (balanced) and RS-423A (unbalanced) electrical implementation of RS-449.

Table 1-1. HP 10342B Specifications and Operating Characteristics (Continued)

Synchronous Data	
Data Transfer Rates (bits/second)	To 72 k bits/second
Bits per Character	6, 7, or 8
Data Format	Captures characters transmitted in character-oriented protocols (COP) with data transmission in one of the following formats: 6-bit transcode using sync character 3AH 7 or 8-bit ASCII using sync character 16H 8-bit EBCDID using sync character 32H Odd, even, or no parity Captures bytes transmitted in bit-oriented protocols (BOP) with data transmitted as 8-bit ASCII or 8-bit EBCDIC.

Table 1-1. HP 10342B Specifications and Operating Characteristics (Continued)

General Characteristics			
	RS-232C/V.24	RS-449	HP-IB
Signals Monitored	TX (BA) RX (BB) RTS (CA) CTS (CB) DSR (CC) DTR (CD) CD (CF)	(SD) (RD) (RS) (CS) (DW) (TR) (RR)	DIO1-8 IFC ATN SRQ REN EOI DAV NRFD NDAC
Signal Loading	One Standard Load	One Standard	1 LS TTL load

Maximum Power Required	0.65 A at +5 VDC, supplied by the logic analyzer.
Accessories Supplied	RS-232C/V.24 ribbon cable 1-0.75 m (2.48 ft). RS-446 ribbon cable 1-0.75 m (2.48 ft) HP-IB ribbon cable 1-0.75 m (2.48 ft)
Accessories Required	HP 10342B and HP 10269C
Logic Analyzer Required	HP 1650A, HP 1651A, or HP 16510A
Number of Probes Required	Two probes for state analysis and/or two probes for timing analysis.

Table 1-1. HP 10342B Specifications and Operating Characteristics (Continued)

General Information	
Inputs	Three provided: RS-232C/(V.24), RS-449, and HP-IB.
Outputs:	Three mini-probe sockets can be connected internally to any of the input lines via jumper wires.
Environmental	
Temperature:	
Operating	0 to 55 degrees C (+32 to +131 degrees F)
Non-operating	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude:	
Operating	up to 4600 m (15,000 ft).
Non-operating	up to 15,300 m (50,000 ft).
Humidity:	90% non-condensing. Avoid sudden, extreme temperature changes that could cause condensation within the instrument.

Equipment Supplied

Equipment supplied with the HP 10342B consists of the following:

* One HP 10342B Preprocessor Module
* One 0.75 meter (2.5 ft) HP-IB ribbon cable
* One 0.75 meter (2.5 ft) RS-232C/V.24 ribbon cable
* One 0.75 meter (2.5 ft) RS-449 ribbon cable
* One 16-pin jumper cable
* 20 jumper wires
* HP 10269B Overlay
* This operating manual

Minimum Equipment Required

The following is a list of the minimum equipment required for a system using the HP 10342B Bus preprocessor.

* HP 1650A, HP 1651A, or HP 16510A Logic Analyzer
* HP 10269C General Purpose Probe Interface
* HP 10342B Bus Preprocessor

2 Hardware Information

Introduction

This chapter contains information about the hardware supplied with the HP 10342B Bus Preprocessor. Inspection, power requirements, maintenance, and setup of the logic analyzer system are some of the subjects covered.

Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or a defect, or if the instrument does not operate, notify your nearest Hewlett-Packard Sales and Service Office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as Hewlett-Packard. Keep the shipping materials for inspection by the carrier.

Power Requirements

The HP 10342B draws power (+5 V) through the analyzer cables of the HP 1650A/51A or HP 16510A Logic Analyzer. It draws approximately 0.65 amps.

Operator Maintainance

The only instrument maintenance an operator needs to perform is to keep the instrument clean. Caution must be used in the selection of cleaning agents. Use a mild soap and water solution. Harsh soaps and solvents could damage the painted finish.

CAUTION

Be careful when cleaning the panel of the instrument. Soap and solvents could damage parts or contaminate circuitry. It is better to apply cleaning solutions to a cloth and wipe the panel, than to wet the surface directly.

CAUTION

Do not use chemical cleaning agents or abrasive cleaners that could damage plastic parts. Recommended cleaning agents are isopropyl alcohol or a 1% solution of mild detergent in water.

Testing and Troubleshooting

There are no established field testing procedures for the HP 10342B. The HP 10342B is part of the Blue-Stripe Exchange program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. If your instrument is inoperative contact the nearest Hewlett-Packard Sales and Service Office for assistance.

Replaceable Parts

Since the HP 10342B is part of the Blue Stripe board exchange program, the only replaceable parts are the major parts and cabling. These are listed in table 2-1.

Table 2-1. Replaceable Parts

Quantity	Description	HP Part Number
1	HP 163X Software Disc	10342-13012
1	HP 165X Software Disc	10342-13017
1	HP-IB Cable	10342-61603
1	RS-232-C Cable	10342-61601
1	RS-449 Cable	10342-61602
1	Probe Interface Overlay	10342-94301
1	16-pin Jumper Cable	10342-61604
20	Jumper wire	8120-4665
1	PC Board	10342-66501
1	Top cover	10342-04104
1	Bottom plate	10342-04102
12	4-40 Flathead screw	2200-0512
2	Captive screw	1390-0393
2	Retaining ring	0510-0952

Schematics

The following information is supplied to help the user understand how the HP 10342B impacts timing measurements of serial bus signals and is not intended for troubleshooting an inoperative instrument.

Serial Input Circuits

The input circuitry for one signal from each of the RS-232 and RS-449 buses is shown in figure 2-1. The inputs for the other signals are identical. Both inputs are buffered and supplied to open-collector drivers. The output of an RS-232 driver is wire-ORed with the output of the corresponding RS-449 driver and the line is pulled up to +5 V.

The RS-232 line receiver has a threshold connection which is connected to ground through 470 pF. This supplies noise immunity for RS-232 signals.

Probing for timing analysis for RS-232 and RS-449 is done after the line receivers. These receivers invert the input signals.

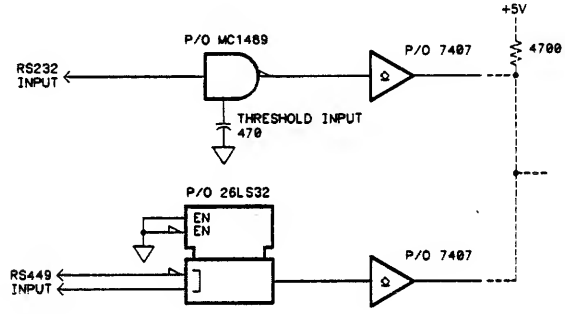


Figure 2-1. Serial Input Circuitry

Serial Timing Connections

An overall view of the timing connections is shown in figure 2-2. The RS-232 and RS-449 input circuitry (previously covered) are represented by their respective blocks.

The three synchronous clocks from the buses are multiplexed with the two asynchronous clocks generated in the HP 10342B in order to provide one transmit and one receive clock. Clock selection depends on the internal and front-panel switch settings. The two selected clocks are used by the SIO and also sent to J6 where they join the buffered and inverted serial signals for connection to the logic analyzer timing inputs.

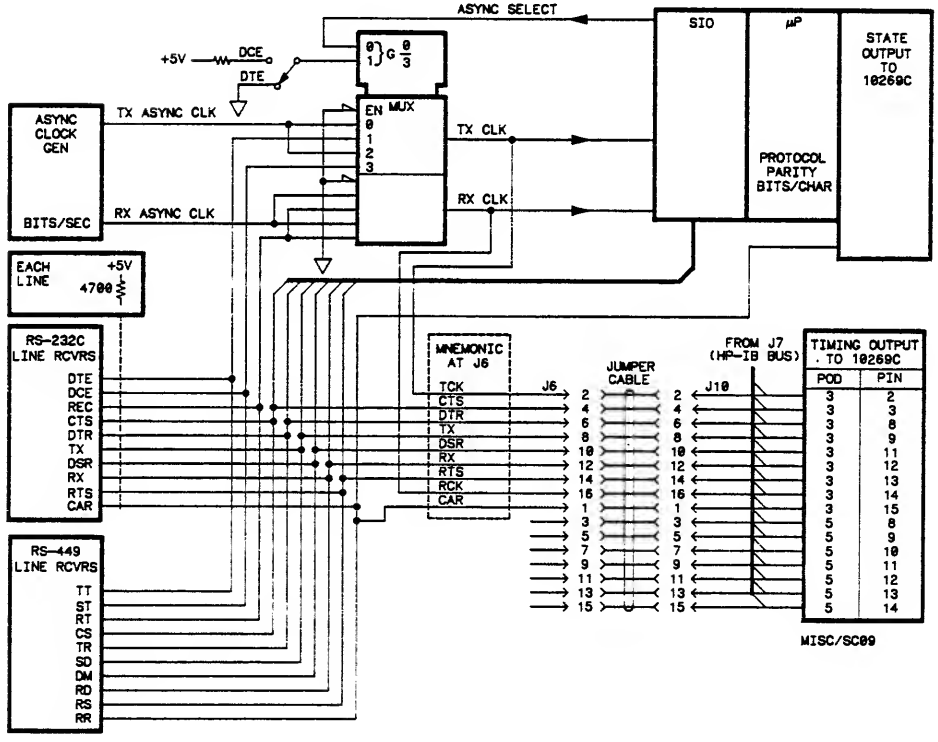


Figure 2-2. Serial Timing Circuitry

3 Software Information

Introduction

This chapter contains information about the software on the disc labeled "HP-IB, RS-232C, and RS-449 Inverse Assemblers for use with the HP 1650A, HP 1651A, and HP 16510A." Two types of files are supplied on this disc, configuration files and inverse assembler files. The configuration files set up the logic analyzer to capture the information from the bus, and load the inverse assembler file. The inverse assembler file is the software routine that decodes the operations of the bus.

Table 3-1 is a list of the files provided with the HP 10342B for use with the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers.

Table 3-1. Software File List

Filename	Filetype	File Description
CHPIB_51	1650/1_config	HPIB CONFIG FOR HP 1651A
CHPIB_I	1650/1_config	HPIB CONFIG FOR 1650A/510A
CRS232_51	1650/1_config	RS232 CONFIG FOR HP 1651A
CRS232_I	1650/1_config	RS232 CONFIG FOR 1650A/510A
CRS449_51	1650/1_config	RS449 CONFIG FOR HP 1651A
CRS449_I	1650/1_config	RS449 CONFIG FOR 1650A/510A
IHPIB_I	inverse_assem	HPIB IA FOR INTERFACE
IRS232_I	inverse_assem	RS232 IA FOR INTERFACE
IRS449_I	inverse_assem	RS449 IA FOR INTERFACE

Copying Files

As soon as possible after receiving your instrument, you should copy your disc. Use the copy and keep the original as a backup.

HP 1650A/51A

On HP 1650A/51A logic analyzers files are copied with the I/O Disc Operations menu. You can copy HP 1650A/51A executable programs, configuration files, and inverse assemblers from one disc to another.

To use the I/O Operations menu to "Copy" files or "Duplicate Discs," configure the menu with the same disc procedures described in the *HP 1650A/51A Front-Panel Operation Reference* manual.

Once the disc operation has been configured, press EXECUTE to copy a file or duplicate a disc. When the operation has been completed, the logic analyzer will display the filename, file type, and description of all files transferred to the new disc.

HP 16510A

For the HP 16510A Logic Analyzer, files are copied with the Front or Rear Disc menu. You can copy HP 16510A executable programs, configuration files, and inverse assemblers from one disc to another.

To use the Front or Rear disc menu to "Copy" files or "Duplicate Discs," configure the menu with the same disc procedures described in the *HP 16500A Logic Analysis System Reference* manual.

Once the disc operation has been configured, press EXECUTE to copy a file or duplicate a disc. When the operation has been completed, the logic analyzer will display the filename, file type, and description of all files transferred to the new disc.

4 HP-IB Bus Preprocessing

Introduction

The HP-IB is the Hewlett-Packard implementation of IEEE Standard 488-1978. The HP-IB is a parallel bus with eight data lines, three handshake lines and five control lines. A brief overview of HP-IB is given in appendix A.

Preprocessor Function

The function of the HP 10342B when monitoring the HP-IB is to connect onto the bus, buffer the lines, provide easy connection to the logic analyzer, set up the logic analyzer menus, and inverse assemble captured data. The HP 10342B can monitor the state of all the HP-IB signal lines. On the HP 1650A and HP 16510A all 16 status and control lines can be monitored for timing information. On the HP 1651A, eight status and control lines can be monitored.

The HP 10342B allows you to either mass-connect the HP-IB lines up to timing channels or individually connect the lines with jumper wires provided. Timing channels are connected directly to the HP-IB without buffering.

Additionally, any HP-IB line can be connected, unbuffered, to one of the three HP 10342B front-panel outputs provided. These can be used for connecting to an oscilloscope.

Equipment Required

The minimum equipment necessary to use the HP 10342B Bus Preprocessor is as follows:

* HP 1650A, HP 1651A, or HP 16510A Logic Analyzer
* HP 10269C Probe Interface
* HP 10342B Bus Preprocessor

Setting Up the HP 10342B

Note

The HP 10342B comes from the factory set up for processing HP-IB, therefore some of the following instructions may be redundant if the HP 10342B is being used for the first time.

1. On the HP 10342B, connect the ribbon jumper cable from J7 to J9. All 16 possible timing channels are connected when the jumper cable is used (see figure 4-1).

   If you use the single jumper wires to connect the timing signals, be sure to connect them to corresponding pins of J7 and J9 or the data captured will not match the HP 1650A/51A or HP 16510A setup provided on disc. You will then need to change the HP 1650A/51A or HP 16510A Timing Format Specification menu to match your hookup.

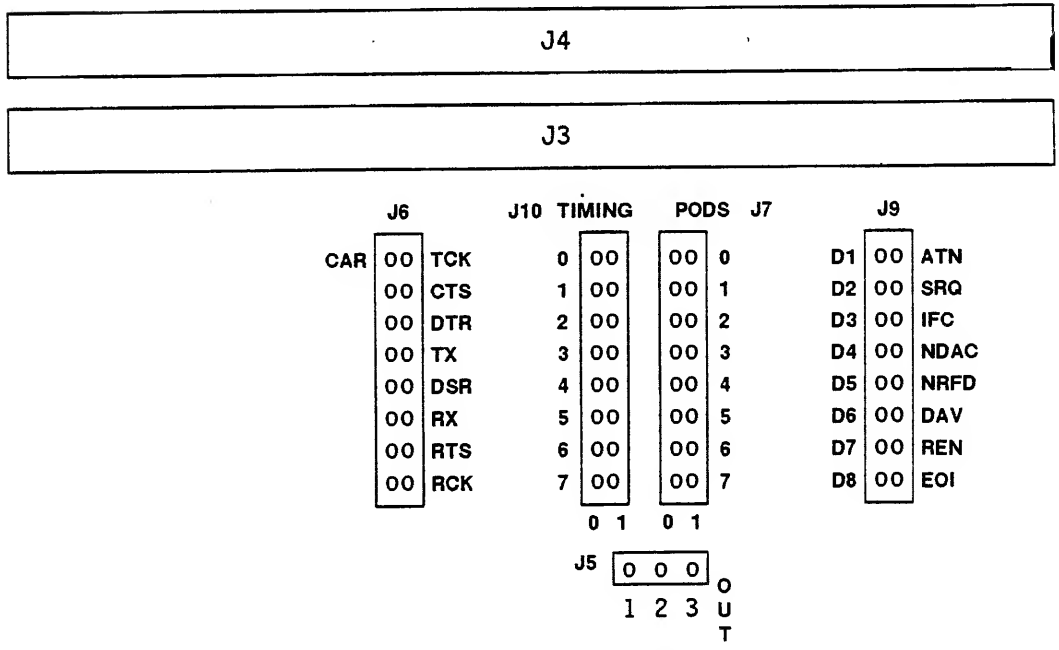


Figure 4-1. HP-IB Timing Connector Locations

2. If you want to connect any data or control lines to the front-panel outputs, use the small jumper wires to connect the pins from J10 to the pins of J5 (see figure 4-1). When the mass-connect jumper cable is used, the signals at J10 correspond to the mnemonics at J9.

   For example, connect ATN to front-panel Output 1 by connecting a jumper between J10 pod 1 pin 0 (top right) and J5 pin 1.

Connecting the HP 10342B to the HP 10269C

1. Once all the connections are made, install the HP 10342B on the bottom of the HP 10269C (see figure 4-2).
2. Insert the free end of the HP 10342B in the slots of the HP 10269C.
3. Connect the two 60-pin cables from the HP 10269C to the connectors on the HP 10342B.
4. Fold the HP 10342B into the bottom of the HP 10269C and fasten the HP 10342B to the HP 10269C with the two captive screws.

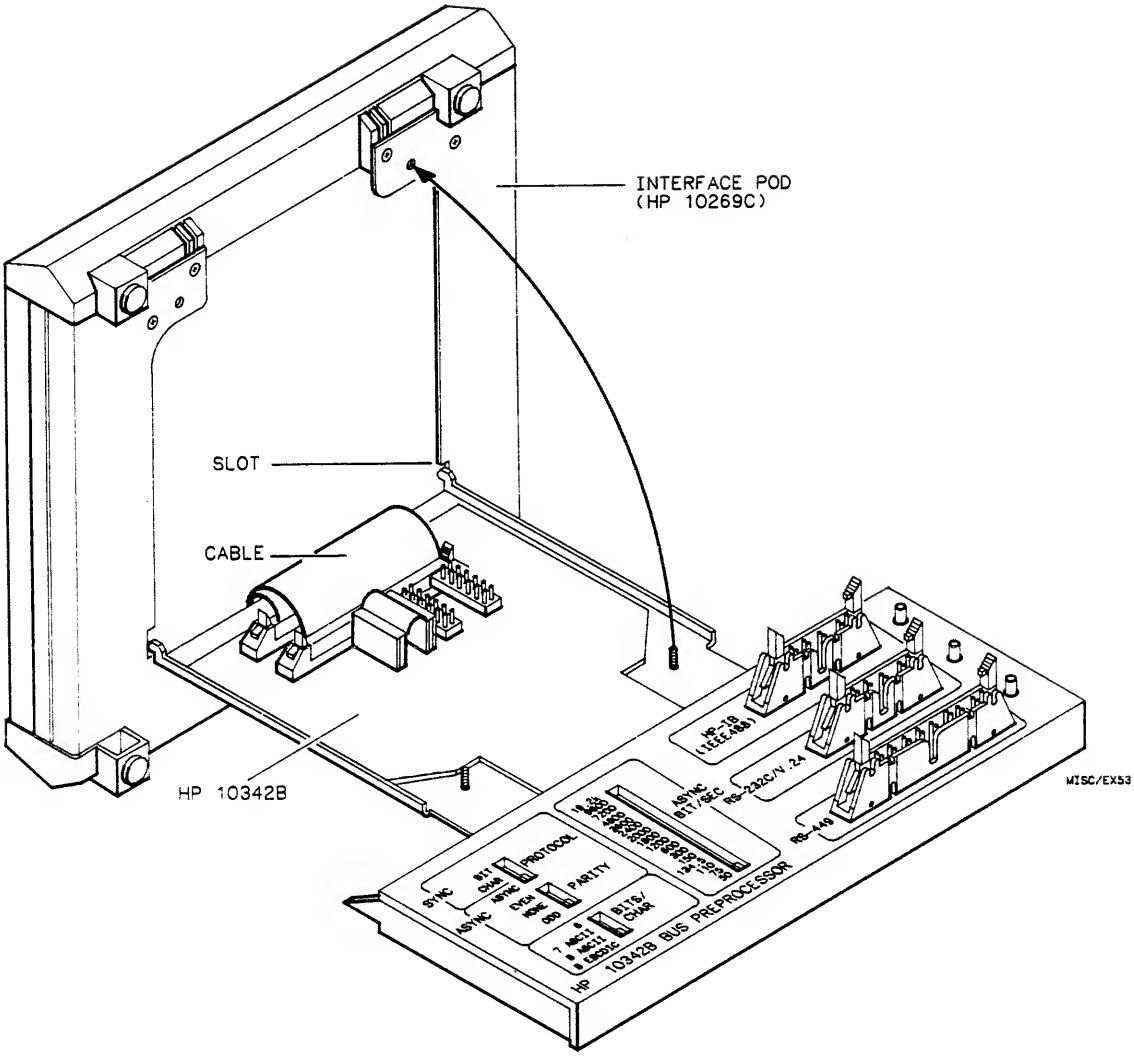


Figure 4-2. Installing the HP 10342B in the HP 10269C

Setting Up the HP 10342B Front Panel

The front-panel switches are used for serial data preprocessing and have no function in preprocessing the HP-IB.

Connecting to the HP 10269C

When using the HP 1650A or HP 16510A connect the logic analyzer probes as follows:

HP 1650A and HP 16510A Probes	(into)	HP 10269C Connector
2		2
3		3
5		5

Since the HP 1651A only has two probes, these probes must be hooked up differently than shown above. To use the HP 10342B with the HP 1651A, connect up the probes as follows.

HP 1651A Probes	(into)	HP 10269C Connector
1		2
2		3

Timing analysis on HP-IB with the HP 1651A is limited to the 8 status and handshake lines.

Setting Up the System

1. Connect the HP-IB ribbon cable between the HP-IB bus to be monitored and the HP-IB connector on the HP 10342B.

2. Turn on power for all equipment involved. The logic analyzer will come up in the System Configuration menu.

Setting Up the Analyzer from the Disc

1. Install the flexible disc labeled "HP-IB, RS-232C, and RS-449 Inverse Assembler for use with HP 1650A, HP 1651A, and HP 16510A" in the front disc drive of the logic analyzer.

2. Select one of the following menus:

   * For the HP 1650A/51A, select the Disc Operations menu;

   * For the HP 16510A, select the System Front Disc menu.

3. Configure the menu to "Load" the analyzer with the configuration file "CHPIB_I" for the HP 1650A or HP 16510A. If you are using an HP 1651A, load the configuration file "CHPIB_51."

4. Execute the load operation to load the file into the HP 1650A, HP 1651A, or HP 16510A.

Accumulating Data

Press RUN and, as soon as a clock is available on the bus, the logic analyzer will begin to accumulate data.

Note

The logic analyzer will flash "Warning Slow Clock" when data is no longer being transmitted across the bus. If you press STOP at this point, the end of the data stream will be displayed.

Signal Connections

The HP 10342B monitors all HP-IB lines for state information. Eight or 16 lines (depending on the logic analyzer) can be monitored for timing information. Table 4-1 lists the HP-IB signals and connections for the HP 1650A/51A and HP 16510A Logic Analyzers.

Table 4-1. Logic Analyzer to HP-IB Signal Connections for the HP 1650A/51A and HP 16510A

	State		Timing	
HP-IB Line	HP 10269C Pod	Pin	HP 10269C Pod	Pin
DAV	2	CLK	-	-
DIO1	2	9	3	15
DIO2	2	10	5	8
DIO3	2	11	5	9
DIO4	2	12	5	10
DIO5	2	13	5	11
DIO6	2	14	5	12
DIO7	2	15	5	13
DIO8	3	0	5	14
PAR POLL**	3	CLK	-	-
ATN	2	0	3	2
EOI	2	1	3	14
REN	2	2	3	13
IFC	2	3	3	8
SRQ	2	4	3	3
NDAC	2	5	3	9
DAV	2	6	3	12
NRFD	2	7	3	11

** Parallel Poll is available but not activated (see "Clocks" on page 4-9).

Clocks

Two clocks are provided to the logic analyzer. These clocks can be ORed to clock data.

DAV

DAV, Data Valid, is brought out at HP 10269C pod connector 2. Logic analyzer POD 2 is connected there, providing DAV as the K Clock. The logic analyzer clocks data on the negative edge of the K Clock.

Parallel Poll

The Parallel Poll clock is brought out at HP 10269C pod connector 3. This is the Clock at logic analyzer POD 3. The PAR POLL clock is ANDed from the EOI and ATN lines of the HP-IB.

The IEEE Standard 488 defines the Parallel Poll as requiring the EOI and ATN lines to be true for 2 μs to be valid. This timing function is not implemented in the HP 10342B.

The configuration file on the disc does not automatically set up the logic analyzer to clock data on parallel polls. To clock data using the ANDed function of EOI and ATN, go to the State Format Specification menu of the logic analyzer. Add an active low L Clock to the clock field. Remember that only data clocked after the 2 μs specification is a valid parallel poll.

Note

Since the HP 1651A does not have 3 pods, the clock signals are setup as follows:

Signal	Clock Used
DAV	↓J
PPOLL	↓K

Status (STAT) Lines

The State Listing monitors the HP-IB interface management (ATN, EOI, REN, IFC, and SRQ) and handshake (NDAC, DAV, and NRFD) lines under the Status label. Only the interface management lines are used in the inverse assembler. Table 4-2 shows which HP-IB line corresponds to which Status line.

Table 4-2. Status Lines

Status Line	HP-IB Line	Status Line	HP-IB Line
STAT 0	ATN	STAT 4	SRQ
STAT 1	EOI	STAT 5	NDAC
STAT 2	REN	STAT 6	DAV
STAT 3	IFC	STAT 7	NRFD

Cycle Lines

The cycle lines are the HP-IB ATN and EOI lines and are the same as the first two STAT lines. They are displayed in the State Display in their symbol format.

Address (ADDR)

There is an Address (ADDR) label set up in the State Format Specification with no bits assigned to the label. This label must be present when you are using an inverse assembler. If the ADDR label appears on screen, you can go to the State Display menu and move this label off the screen. This label is moved off the screen by the configuration file when the software is loaded.

Setting Up the Analyzer for Timing Analysis

The HP 10342B software automatically configures the logic analyzer for state analysis. The logic analyzer can also perform timing analysis on the HP-IB lines. To set up the logic analyzer for timing analysis, you will need to do the following:

1. In the System menu of the logic analyzer, configure Analyzer 2 to be a Timing Analyzer.

2. For the HP 1650A or HP 16510A, assign pods 3 and 5 to Analyzer 2. You should see a display as shown in figure 4-3.

3. For the HP 1651A, assign pod 2 to Analyzer 2. You should see a display as shown in figure 4-4.

The Format menu will provide a label for each signal.

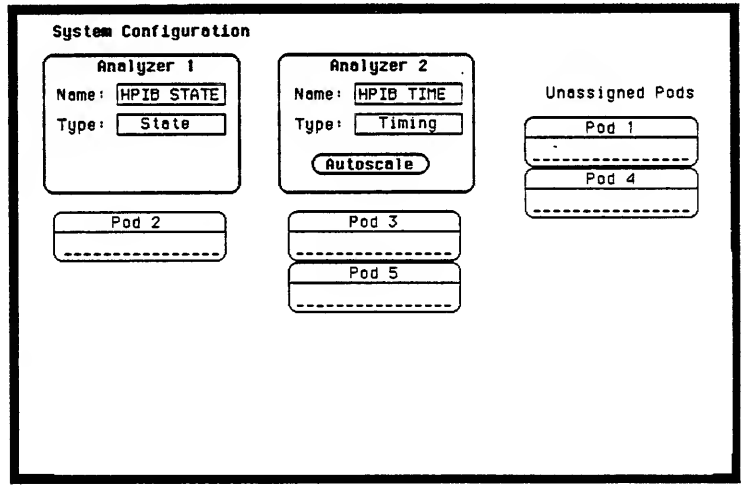


Figure 4-3. Configuration Menu for Timing Analysis with the HP 1650A or HP 16510A

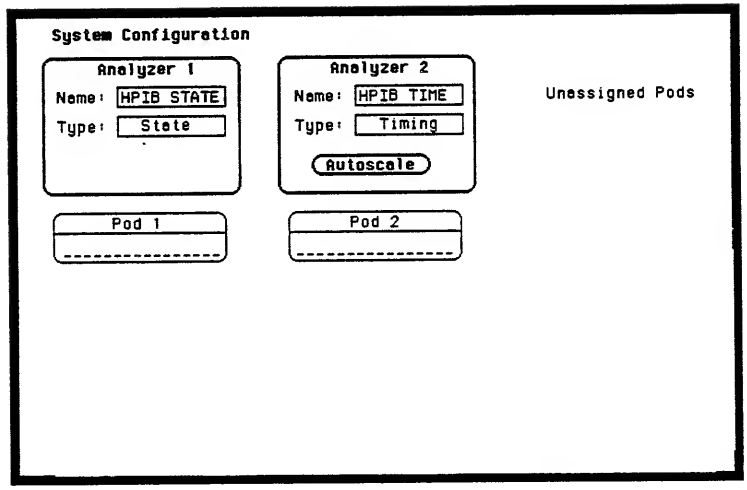


Figure 4-4. Configuration Menu for Timing Analysis with the HP 1651A

5 RS-232-C/V.24 Bus Preprocessing

introduction

The RS-232-C/V.24 is a serial interface with unbalanced data and control lines. A brief overview of RS-232-C/V.24 is given in Appendix C. Several of the serial interfaces are compared in Appendix B. Further references to RS-232-C should be assumed to include CCITT V.24.

Preprocessor Function

The primary function of the HP 10342B is to convert serial data stream to parallel data and status. The HP 10342B monitors five handshake lines and stores their states for each character. Four of the handshake lines are synchronous with the serial controller and one line (carrier detect) is asynchronous but sampled each time a character is output to the logic analyzer.

All lines are buffered at the input to the HP 10342B. The buffers provide one RS-232-C standard load to the bus. Signals are inverted by the buffer circuitry.

The HP 10342B can mass-connect the bus lines to timing channels, or the lines can be individually connected with the jumper wires provided. Timing connections are made to the buffered and inverted signals.

Additionally, any buffered line can be connected to one of the three HP 10342B front-panel outputs provided. These can be used for connecting to an oscilloscope.

Equipment Required

The minimum equipment necessary to use the HP 10342B Bus Preprocessor is as follows:

* HP 1650A, HP 1651A, or HP 16510A Logic Analyzer
* HP 10269C Probe Interface
* HP 10342B Bus Preprocessor

Setting Up the HP 10342B

Note

The HP 10342B comes from the factory set up for processing HP-IB.

1. On the HP 10342B, connect the ribbon jumper cable to the appropriate pins. All 16 possible timing channels are connected when the jumper cable is connected from J6 to J10. Only nine channels are used with RS-232-C processing (see figure 5-1).

   If you use the single jumper wires to connect the timing signals be sure to connect them to corresponding pins of J6 and J10 or the data captured will not match the HP 1650A/51A or HP 16510A setup provided on disc. You would then need to change the HP 1650A/51A or HP 16510A Timing Format Specification menu to match your hook-up.

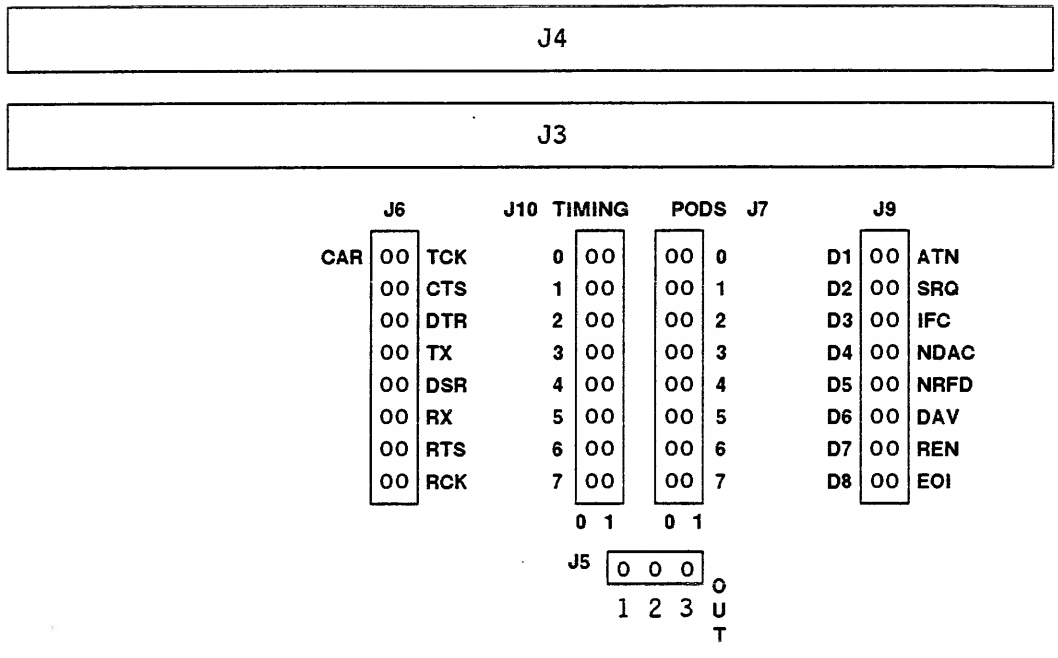


Figure 5-1. RS-232-C Timing Connector Locations

2. If you want to connect any data or control lines to the front-panel outputs, use the single jumper wires to connect pins of J7 to pins of J5 (see figure 5-1). When you are using the mass-connect jumper cable, the signals at J7 correspond to the mnemonics at J6.

   For example, connect TCK to front-panel Output 1 by connecting a jumper between J7 pod 1 pin 0 (top right) and J5 pin 1.

3. Set the DTE/DCE switch (see figure 5-2) to the position corresponding to the desired sync transmit clock. If the transmit clock from the terminal (computer) is desired, use DTE and, if the transmit clock from the modem is desired, use DCE.

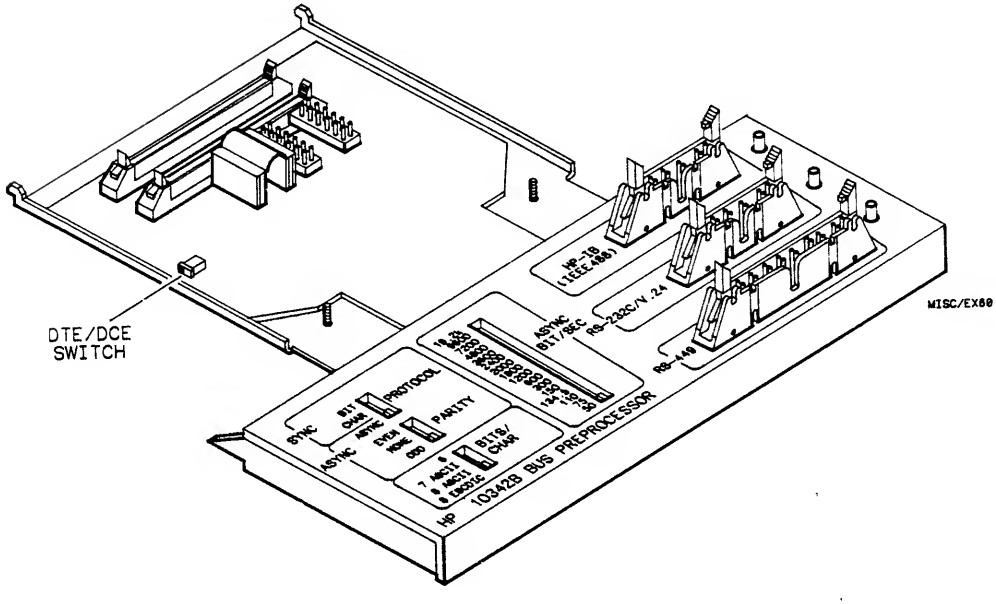


Figure 5-2. DTE/DCE Switch Location

Connecting the HP 10342B to the HP 10269C

1. Once all the connections are made, install the HP 10342B on the bottom of the HP 10269C (see figure 5-3).
2. Insert the free end of the HP 10342B in the slots of the HP 10269C.
3. Connect the two 60-pin cables from the HP 10269C to the connectors on the HP 10342B.
4. Fold the HP 10342B into the bottom of the HP 10269C and fasten the HP 10342B to the HP 10269C with the two captive screws.

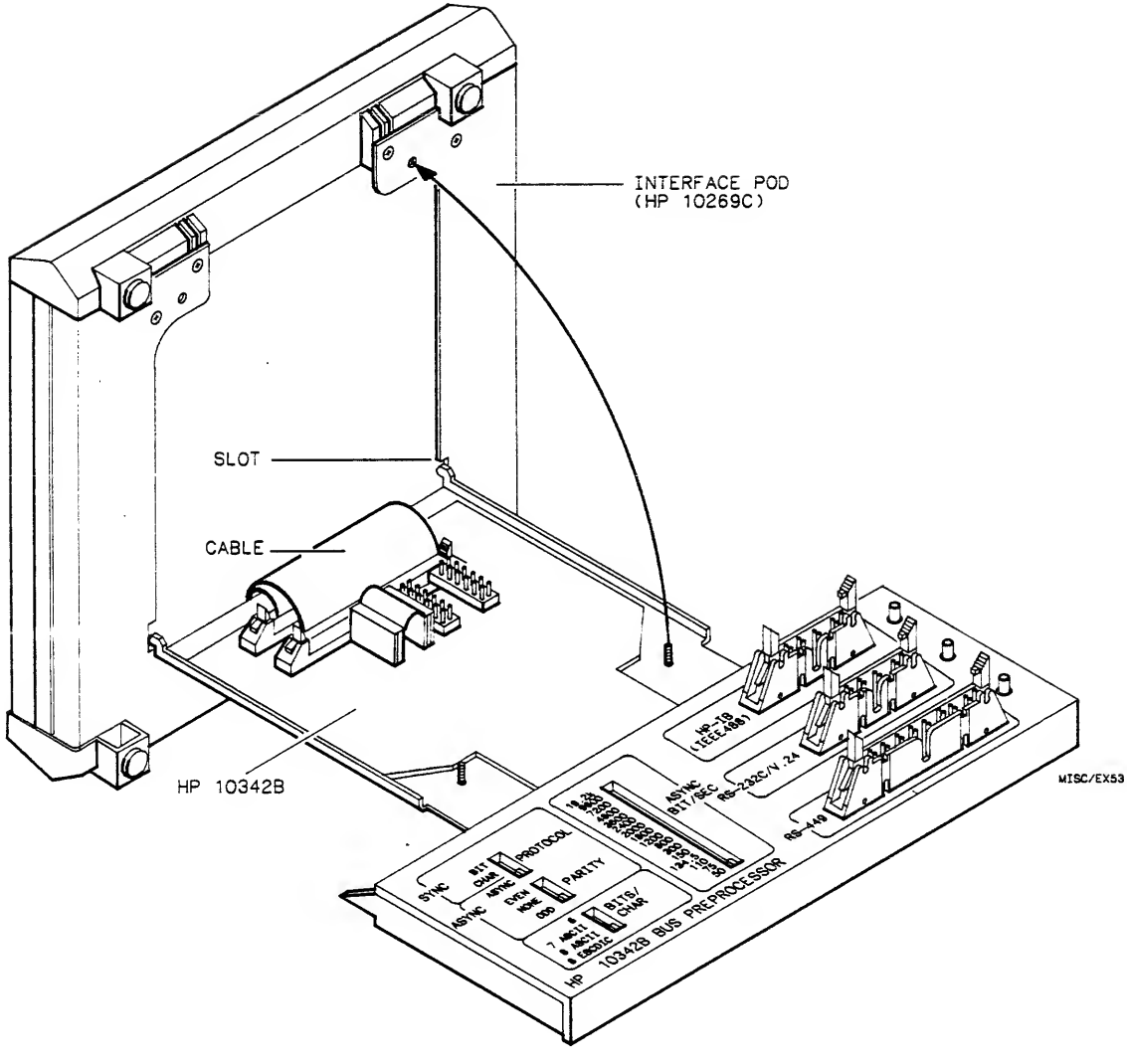


Figure 5-3. Installing the HP 10342B in the HP 10269C

Setting Up the HP 10342B Front Panel

Set the front-panel switches according to the protocol, parity, etc. of the bus you are working with. The HP 10342B needs the proper protocol settings to disassemble the data on the bus.

* In BIT PROTOCOL (BOP, bit oriented synchronous protocol), the only other switch setting that must be made is 8 ASCII or 8 EBCDIC in BITS/CHAR. No other switch settings are relevant because the rest of the protocol is predefined. Clock comes from the external source, either terminal (DTE) or modem (DCE).

* In CHAR PROTOCOL (BCP, byte control synchronous protocol), the PARITY and BITS/CHAR switches must be set so that the HP 10342B knows which characters to sync on. These sync characters are not displayed due to internal processing in the HP 10342B. The clock comes from an external source, either terminal (DTE) or modem (DCE).

* When ASYNChronous is selected, the settings of all other front panel switches are relevant. The clock source is from an internal source ASYNC BITS/SEC.

    1. Set the PARITY to the proper setting.

    2. Set the BITS/CHAR.

    3. Set the ASYNC BITS/SEC.

Note

When transmit or receive data is present a state will be stored. Lack of data, or improper sync characters, results in a slow clock indication from the logic analyzer.

Connecting to the HP 10269C

When using the HP 1650A or HP 16510A, connect the logic analyzer probes as follows:

HP 1650A and 16510A Probes	(into)	HP 10269C Connector
1		1
4		4

Since the HP 1651A only has two probes, this logic analyzer must be hooked up differently than shown above. When you use the HP 1651A with the HP 10342B, connect the logic analyzer probes as follows:

HP 1651A Probes	(into)	HP 10269C Connector
1		1
2		4

Setting Up the System

1. Connect the RS-232 ribbon cable between the bus to be monitored and the RS-232C/V.24 connector on the HP 10342B.

2. Turn on power for all equipment involved. The logic analyzer will come up in the System Configuration menu.

Setting Up the Analyzer from the Disc

1. Install the flexible disc labeled "HP-IB, RS-232C, and RS-449 Inverse Assembler for use with HP 1650A, HP 1651A, and HP 16510A" in the front disc drive of the logic analyzer.

2. Select one of the following menus:

   * For the HP 1650A/51A, select the Disc Operations menu;

   * For the HP 16510A, select the System Front Disc menu.

3. Configure the menu to "Load" the analyzer with the configuration file "CRS232_I" for the HP 1650A or HP 16510A. If you are using an HP 1651A, load the configuration file "CRS232_51."

4. Execute the load operation to load the file into the HP 1650A, HP 1651A, or HP 16510A.

Accumulating Data

Press RUN and, as soon as a clock is available on the bus, the logic analyzer will begin to accumulate data.

Note

The logic analyzer will flash "Warning Slow Clock" when data is no longer being transmitted across the bus. If you press STOP at this point, the end of the data stream will be displayed.

Signal Connections

The HP 10342B provides processed data and status to the logic analyzer state inputs. The timing inputs are buffered from the RS-232-C bus except for TX CLK and RX CLK, which are selected in the HP 10342B.

Table 5-1. Logic Analyzer to RS-232-C Signal Connections (HP 1650A/51A and HP 16510A)

State*			Timing		
	HP 10269C			HP 10269C	
Signal	Connector	Pin	Signal	Connector	Pin
Clock	4	CLK	TX CLK**	3	2
			CTS***	3	3
	1	0	DTR***	3	8
	1	1	TX***	3	9
Serial	1	2			
Data	1	3	DSR***	3	11
Converted			RX***	3	12
to	1	4	RTS***	3	13
Parallel	1	5	RX CLK**	3	14
	1	6			
	1	7	CAR***	3	15
TX/RX	1	8			
CC LSB	1	9			
CC MSB	1	10			
CTS	1	11			
DSR	1	12			
RTS	1	13			
DTR	1	14			
CD	1	15			

* Processed through SIO in HP 10342B.

** Clock selected in HP 10342B.

*** Signal from buffered RS-232-C lines.

Clock

One clock is supplied to the logic analyzer from the processor in the HP 10342B. For the HP 1650A and HP 16510A, this clock is provided to pod 4 an is the M Clock. For the HP 1651A, this clock is provided to pod 2 and is the K Clock. The logic analyzer clocks data on the negative edge of the clock.

Data

The Data, at HP 10269C connector 1 (logic analyzer POD 1), is the parallel format of the serial data byte. It has been processed in the SIO (Serial IN/OUT Interface) and microprocessor of the HP 10342B.

Status Byte

The Status Byte, at Connector 1 of the HP 10269C, is provided by the microprocessor in the HP 10342B.

Bit 0 represents whether the data is transmitted (1) or received (0) and is used by the inverse assembler.

Bits 1 and 2, CC LSB and CC MSB, represent front panel settings for BITS/CHAR and are used by the inverse assembler to interpret data.

00 = Normal Character

01 = EBCDIC Character Set

10 = 6-bit Transcode Character Set

11 = Not Used

Bits 3-7 are the handshake signals. They have been processed in the SIO of the HP 10342B and represent the status of the handshake lines for each serial data byte.

Address (ADDR)

There is an Address (ADDR) label set up in the State Format Specification with no bits pod assigned to the label. There is no RS-232-C information in this label. This label must be present when you are using an inverse assembler. If the ADDR label appears on screen you can go to the State Display menu and move it off the screen. This is done automatically by the configuration file when the software is loaded.

Mnemonics

The HP 10342B inverse assembler for RS-232-C uses common mnemonics rather than the mnemonics specified in the EIA Standard. Table 5-2 provides a cross reference.

Table 5-2. RS-232-C Mnemonic Cross Reference

Pin	Mnemonic	
	Common	RS-232-C
2	TX	BA
3	RX	BB
4	RTS	CA
5	CTS	CB
6	DSR	CC
8	CD	CF
15	DCE CLK	DB
17	REC CLK	DD
20	DTR	CD
24	DTE CLK	DA

Sync Characters

The HP 10342B must receive the proper sync characters in order to process data. The SIO is programmed to recognize the standard sync characters for the selected character code. If some other sync characters are being sent to the HP 10342B, the logic analyzer will display "Slow Clock."

The transmitted sync character can be seen in only the timing display. The HP 10342B does not provide the sync characters to the state display. Table 5-3 shows the expected sync characters for given character codes.

Table 5-3. Standard Sync Characters

CHAR CODE	SYNC CHAR
6 BIT TRANS	3A3A HEX
7 BIT ASCII	1616 HEX
8 BIT ASCII	1616 HEX
8 BIT EBCDIC	3232 HEX

The SIO recognizes a 16-bit "character word." When observing the sync character data string, take into account the relationship of this word to the idle characteristics of the data line and the parity of the transmitted data.

For example, when observing bit strings on the timing channels of the logic analyzer, note that data is clocked on the rising edge of TX CLK or RX CLK.

As can be seen in figure 5-4, the SIO uses two "bits" from the idle bus to fill out the two "missing" bits of the character. It then uses 2C5BH as a comparison to recognize the sync characters. If the bus does not idle high (idle high is standard), the sync characters will not be recognized.

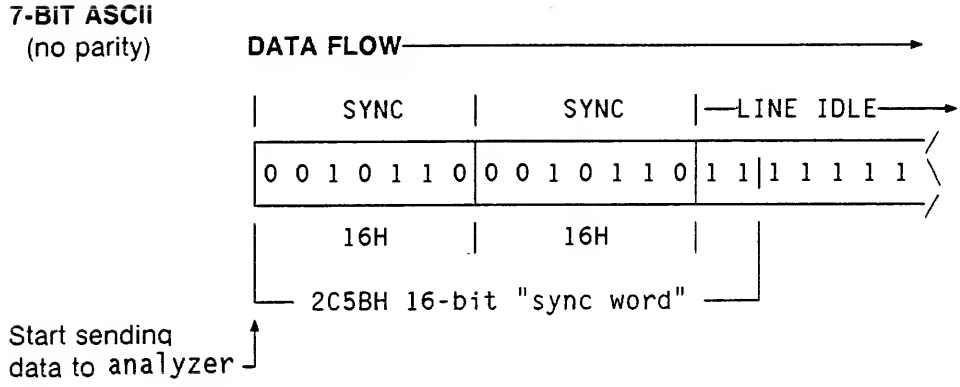


Figure 5-4. 7-Bit ASCII Sync Sequence

In figure 5-5 the sync characters with parity have a longer bit string than the "sync word." The two least significant bits are dropped and the SIO uses 994CH as a comparison to recognize the sync characters.

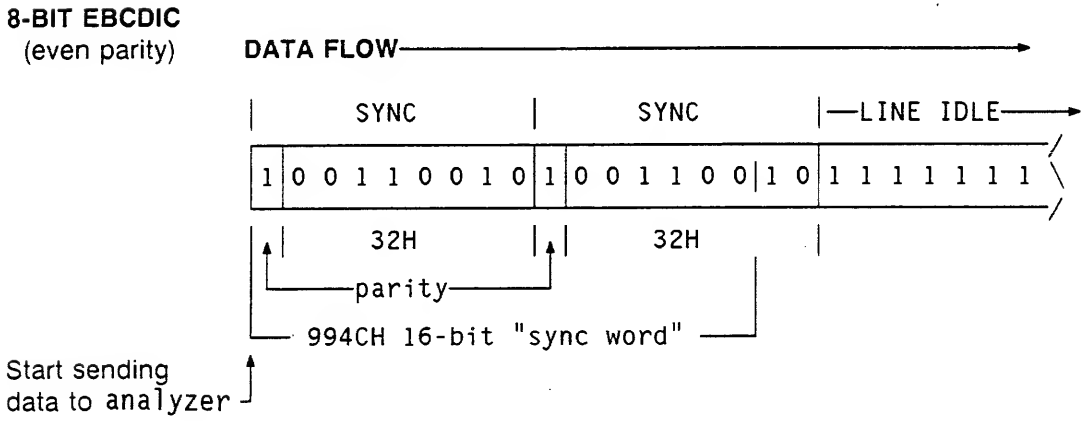


Figure 5-5. 8-Bit EBCDIC Sync Sequence

Block Check Characters

Tha last two characters of the data stream are Block Check Characters (BCC). These characters are actually CRCs and are passed on to the logic analyzer as data. However, they have been altered by the SIO and their value is no longer significant.

Setting Up the HP1650A or HP 16510A for Timing Analysis

The HP 10342B software automatically configures the logic analyzer for state analysis. The logic analyzer can also perform timing analysis on the RS-232 lines. To set up the logic analyzer for timing analysis, you will need to do the following:

1. In the Configuration menu of the logic analyzer, configure Analyzer 2 to be a timing analyzer.

2. Assign pod 3 to Analyzer 2. You should see a display as shown in figure 5-6.

3. Connect probe 3 from the logic analyzer to POD 3 on the HP 10269C.

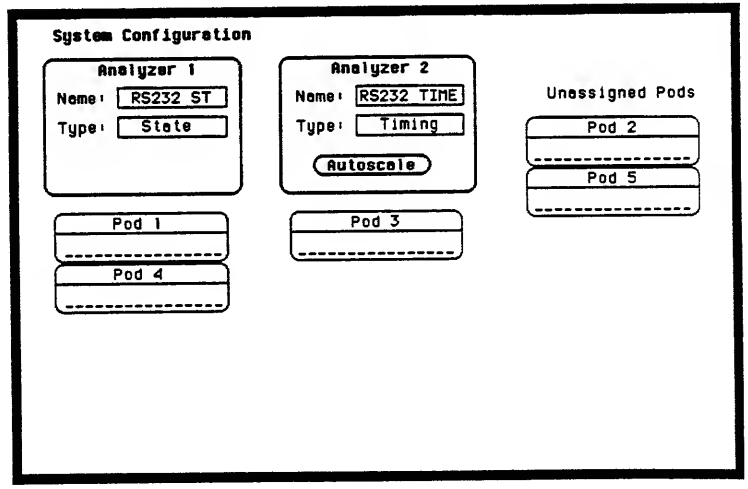


Figure 5-6. Configuration Menu for Timing Analysis with the HP 1650A or HP 16510A

The Format menu will provide a label for each signal.

The following signals are turned off in the Format menu:

RX CLK, TX CLK, RX, TX

To capture these signals with the timing analyzer, turn on the appropriate labels in the Format menu.

Refer to page 5-16 for more information on the timing signals.

Setting Up the HP 1651A for Timing Analysis

The HP 10342B software automatically configures the HP 1651A for state analysis. The logic analyzer can also perform timing analysis on the RS-232C lines. To set up the HP 1651A for timing analysis, you will need to do the following:

1. In the logic analyzer System menu configure Analyzer 2 to be a Timing Analyzer.

2. Assign pod 2 to Analyzer 2. You should see the display as shown in figure 5-7.

3. Move pod 2 from connector 4 to connector 3 on the HP 10269C.

The Format menu of the HP 1651A will provide a label for each signal.

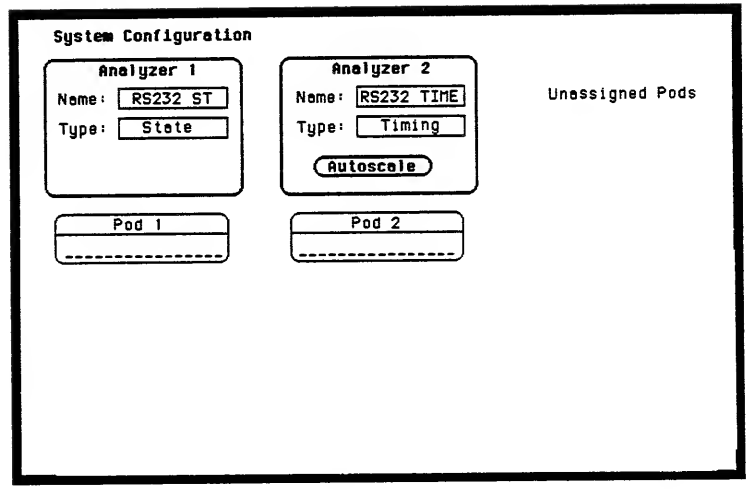


Figure 5-7. Configuration Menu for Timing Analysis with the HP 1651A

Timing Signals

For further information about the timing signals see the "Schematics" section in Chapter 2.

Most timing signals are buffered directly from the RS-232-C bus. The TXCLK and RXCLK are clocks selected in the HP 10342B by the DTE/DCE switch and front-panel setup.

On asynchronous buses, the RX CLK and TX CLK are generated by the HP 10342B circuitry and are not signals sent across RS-232-C.

On synchronous buses, the RX CLK is the REC CLK signal (DD, pin 17). The TX CLK is either the DTE CLK signal (DA, pin 24) or the DCE CLK signal (DB, pin 15), depending on the setting of the DTE/DCE switch on the HP 10342B.

The Carrier Detect (CAR) is also buffered directly from the RS-232-C bus.

The timing signals supplied to the logic analyzer are of the opposite sense to the mark/space definition in the RS-232-C standard (see figure 5-8). The line receivers buffer, invert, and convert the RS-232 signals to TTL. The logic analyzer timing inputs are not designed to handle the +25 V signals specified by RS-232-C, so they are connected to the buffered signals.

Though the timing signals are of the opposite sense to that defined by the RS-232-C specification, they are of the same sense as the signals supplied to the RS-232 line drivers in the DCE. This makes it easier to compare the output (TTL) of the asynchronous receiver/transmitter in the DCE to the TTL signal applied to the SIO in the DTE.

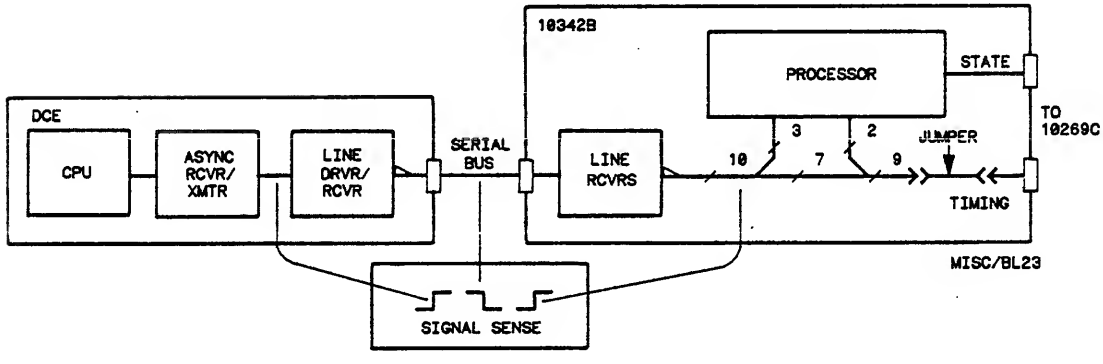


Figure 5-8. Signal Sense Diagram

6 RS-449 Bus Preprocessing

Introduction

The RS-449 is a serial interface with balanced data and control lines. A brief overview of RS-449 is given in Appendix D. Several of the serial interfaces are compared in Appendix B.

Preprocessor Function

The RS-449 has two categories of interchange circuits, Category I and Category II. Category I circuits are balanced high-speed circuits. Category II circuits are low-speed, unbalanced circuits used for secondary functions. The HP 10342B processes only the Category I circuits.

The primary function of the HP 10342B is to convert the serial data stream into parallel data and status. The HP 10342B monitors five handshake lines and stores their states for each character. Four of the handshake lines are synchronous with the serial controller and one line (carrier detect) is asynchronous but sampled each time a character is output to the logic analyzer.

All lines are buffered at the input to the HP 10342B. The buffers provide one RS-449 standard load to the bus. Signals are inverted by the buffer circuitry.

The HP 10342B can mass-connect the bus lines to timing channels, or the lines can be individually connected with the jumper wires provided. Timing connections are made to the buffered and inverted signals.

Additionally, any buffered line can be connected to one of the three HP 10342B front-panel outputs provided. These can be used for connection to an oscilloscope.

Equipment Required

The minimum equipment necessary to use the HP 10342B Bus Preprocessor is as follows:

* HP 1650A, HP 1651A, or HP 16510A Logic Analyzer
* HP 10269C Probe Interface
* HP 10342B Bus Preprocessor

Setting Up the HP 10342B

Note

The HP 10342B comes from the factory set up for processing HP-IB.

1. On the HP 10342B, connect the ribbon jumper cable to the appropriate pins. All 16 possible timing channels are connected when the jumper cable is connected from J6 to J10. Only nine channels are used with RS-449 processing (see figure 6-1).

   If you use the single jumper wires to connect the timing signals, be sure to connect them to corresponding pins of J6 and J10 or the data captured will not match the HP 1650A/51A or HP 16510A setup provided on disc. You will need to change the HP 1650A/51A or HP 16510A Timing Format Specification menu to match your hook-up.

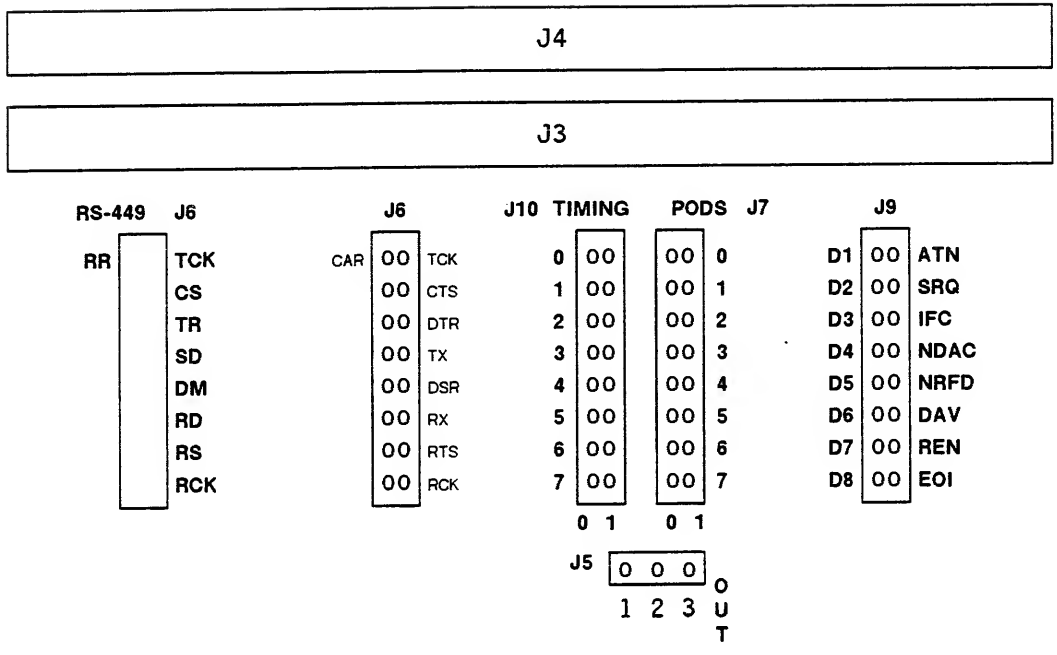


Figure 6-1. Timing Connector Locations

2. If you want to connect any data or control lines to the front-panel outputs, use the single jumper wires to connect pins of J7 to pins of J5 (see figure 6-1). When you're using the mass-connect jumper cable, the signals at J7 correspond to the mnemonics at J6.

   For example, connect TCK to front-panel Output 1 by connecting a jumper between J7 pod 1 pin 0 (top right) and J5 pin 1.

3. Set the DTE/DCE switch (left side of PC board) to the position corresponding to the desired sync transmit clock. If the transmit clock from the terminal (computer) is desired, use DTE and, if the transmit clock from the modem is desired, use DCE.

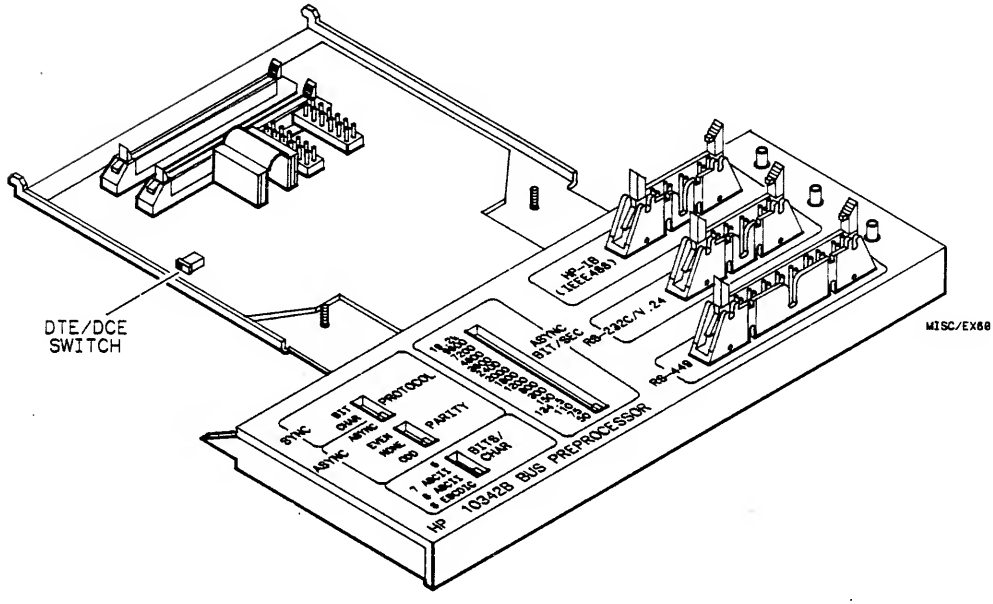


Figure 6-2. DTE/DCE Switch Location

Connecting the HP 10342B to the HP 10269C

1. Once all the connections are made, install the HP 10342B on the bottom of the HP 10269C (see figure 6-3).
2. Insert the free end of the HP 10342B in the slots of the HP 10269C.
3. Connect the two 60-pin cables from the HP 10269C to the connectors on the HP 10342B.
4. Fold the HP 10342B into the bottom of the HP 10269C and fasten the HP 10342B to the HP 10269C with the two captive screws.

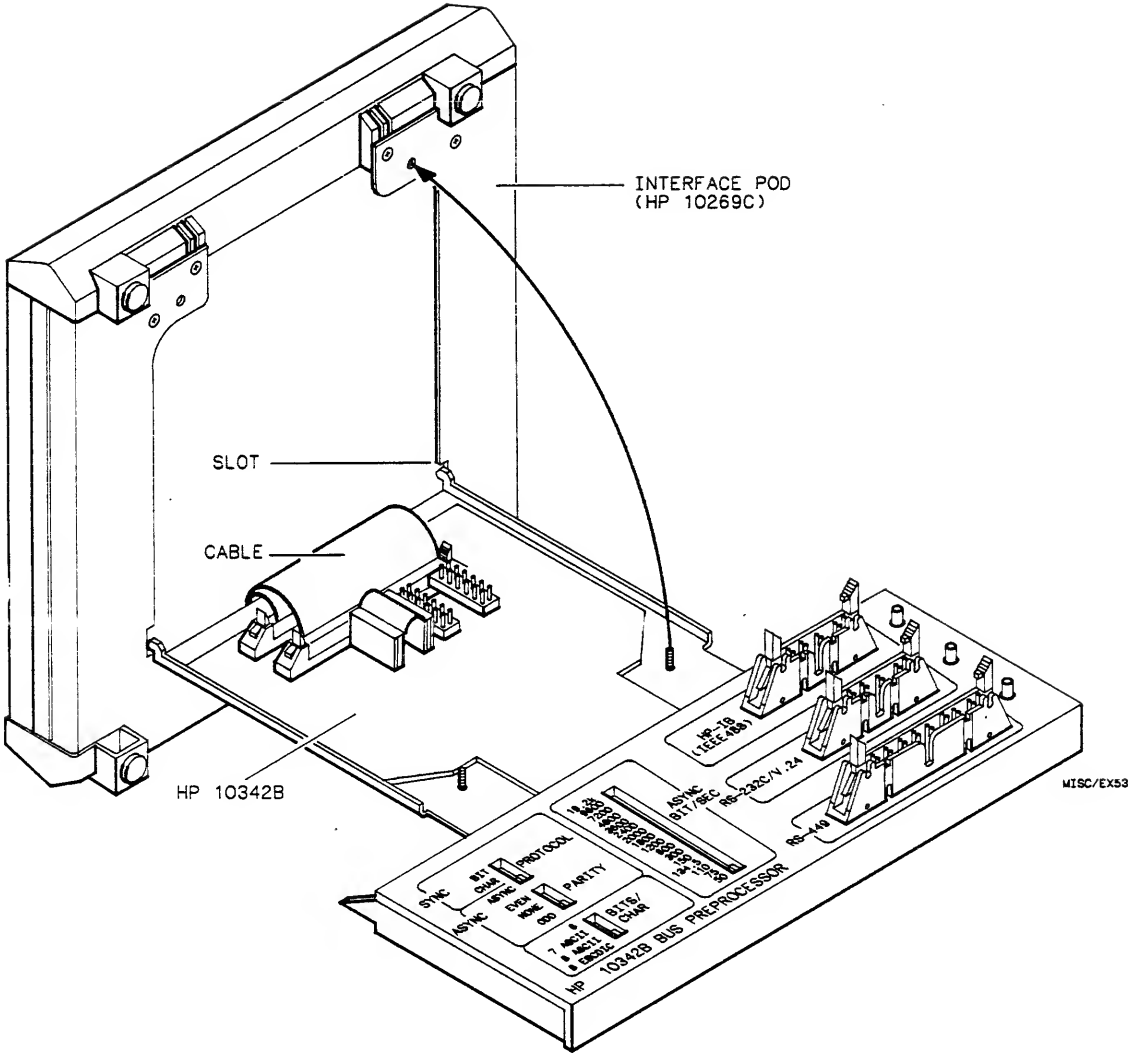


Figure 6-3. Installing the HP 10342B in the HP 10269C

Setting Up the HP 10342B Front Panel

Set the front-panel switches according to the protocol, parity, etc. of the bus you are working with. The protocol must be set correctly for the HP 10342B to disassemble the data on the bus.

* In BIT PROTOCOL (BOP, bit oriented synchronous protocol), the only other switch that must be set is 8 ASCII or 8 EBCDIC in BITS/CHAR. No other switch settings are relevant because the rest of the protocol is predefined. Clock comes from the external source, either terminal (DTE) or modem (DCE).

* In CHAR PROTOCOL (BCP, byte control synchronous protocol), the PARITY and BITS/CHAR switch settings must be set so that the HP 10342B knows which characters to sync on. These characters are not displayed due to internal processing in the HP 10342B. Clock comes from the external source, either terminal (DTE) or modem (DCE).

* When ASYNChronous is selected, the settings of all other front-panel switches are relevant. The clock source is from the internal source, ASYNC BITS/SEC. To select ASYNChronous:

  1. Set the PARITY to the proper setting.

  2. Set the BITS/CHAR.

  3. Set the ASYNC BITS/SEC.

Note

When transmit or receive data is present a state will be stored. Lack of data results in a slow clock indication from the logic analyzer.

Connecting to the HP 10269C

When using the HP 1650A or HP 16510A connect the logic analyzer probes as follows:

HP 1650A and HP 16510A Probes	(into)	HP 10269C Connector
1		1
4		4

Since the HP 1651A only has two probes, this logic analyzer must be hooked up differently than shown above. To use the HP 10342B with the HP 1651A, connect up the probes as follows.

HP 1651A Probes	(into)	HP 10269C Connector
1		1
2		4

Setting Up the System

1. Connect the RS-449 ribbon cable between the bus to be monitored and the RS-449 connector on the HP 10342B.

2. Turn on power for all equipment involved. The logic analyzer will come up in the System Configuration menu.

Setting Up the Analyzer from the Disc

1. Install the flexible disc labeled "HP-IB, RS-232C, and RS-449 Inverse Assembler for use with HP 1650A, HP 1651A, and HP 16510A" in the front disc drive of the logic analyzer.

2. Select one of the following menus:

   * For the HP 1650A/51A, select the Disc Operations menu;

   * For the HP 16510A, select the System Front Disc menu.

3. Configure the menu to "Load" the analyzer with the configuration file "CRS449_I" for the HP 1650A or HP 16510A. If you are using an HP 1651A, load the configuration file "CRS449_51."

4. Execute the load operation to load the file into the HP 1650A, HP 1651A, or HP 16510A.

Accumulating Data

Press RUN and, as soon as a clock is available on the bus, the logic analyzer will begin to accumulate data.

Note

The logic analyzer will flash "Warning Slow Clock" when data is no longer being transmitted across the bus. If you press STOP at this point, the end of the data stream will be displayed.

Signal Connections

The HP 10342B provides processed data and status to the logic analyzer state inputs.

Table 6-1. Logic Analyzer to RS-449 Signal Connections (HP 1650A/51A and HP 16510A)

State*			Timing		
	HP 10269C			HP 10269C	
Signal	Connector	Pin	Signal	Connector	Pin
Clock	4	CLK	TX CLK**	3	2
			CS***	3	3
	1	0	TR***	3	8
	1	1	SD***	3	9
Serial	1	2			
Data	1	3	DM***	3	11
Converted			RD***	3	12
to	1	4	RS***	3	13
Parallel	1	5	RX CLK**	3	14
	1	6			
	1	7	RR***	3	15
TX/RX	1	8			
CC LSB	1	9			
CC MSB	1	10			
CS	1	11			
DM	1	12			
RS	1	13			
TR	1	14			
RR	1	15			

* Processed through SIO in HP 10342B.

** Clock selected in HP 10342B.

*** Signal from buffered RS-449 lines.

Clock

One clock is supplied to the logic analyzer from the microprocessor in the HP 10342B. For the HP 1650A and HP 16510A, this clock is provided to pod 4 and is the M Clock. For the HP 1651A, this clock is provided to pod 2 and is the K Clock. The logic analyzer clocks data on the negative edge of the clock.

Data

The Data, at HP 10269C connector 1 (logic analyzer POD 1), is the parallel format of the serial data byte. It has been processed in the SIO (Serial IN/OUT interface) and microprocessor of the HP 10342B.

Status Byte

The Status Byte, at connector 1 of the HP 10269C, is provided by the microprocessor in the HP 10342B.

Bit 0 represents whether the data is transmitted (1) or received (0) and is used by the inverse assembler.

Bits 1 and 2, CC LSB and CC MSB, represent front-panel settings for BITS/CHAR and are used by the inverse assembler to interpret data.

00 = Normal Character

01 = EBCDIC Character Set

10 = 6-bit Transcode Character Set

11 = Not Used

Bits 3-7 are the handshake signals. They have been processed in the SIO of the HP 10342B and represent the status of the handshake lines for each serial data byte.

Address (ADDR)

There is an Address (ADDR) label set up in the State Format Specification with no bits from a pod assigned to the label. There is no RS-449 information in this label. This label must be present when you are using an inverse assembler. If the ADDR label appears on screen, you can go to the State Display menu and move it off the screen. This is done automatically by the configuration file when the software is loaded.

Sync Characters

The HP 10342B must receive the proper sync characters in order to process data. The SIO is programmed to recognize the standard sync characters for the selected character code. If some other sync characters are being sent to the HP 10342B, the logic analyzer will display "Slow Clock".

The transmitted sync character can be seen in only the timing display. The HP 10342B does not provide the sync characters to the state display. Table 6-2 shows the expected sync characters for given character codes.

Table 6-2. Standard Sync Characters

CHAR CODE	SYNC CHAR
6 BIT TRANS	3A3A HEX
7 BIT ASCII	1616 HEX
8 BIT ASCII	1616 HEX
8 BIT EBCDIC	3232 HEX

The SIO recognizes a 16-bit "character word". When observing the sync character data string, take into account the relationship of this word to the idle characteristics of the data line and the parity of the transmitted data.

For example, when observing bit strings on the timing channels of the logic analyzer, note that data is clocked on the rising edge of TX CLK or RX CLK.

As can be seen in figure 6-4, the SIO uses two "bits" from the idle bus to fill out the two "missing" bits of the character. It then uses 2C5BH as a comparison to recognize the sync characters. If the bus does not idle high (idle high is standard), the sync characters will not be recognized.

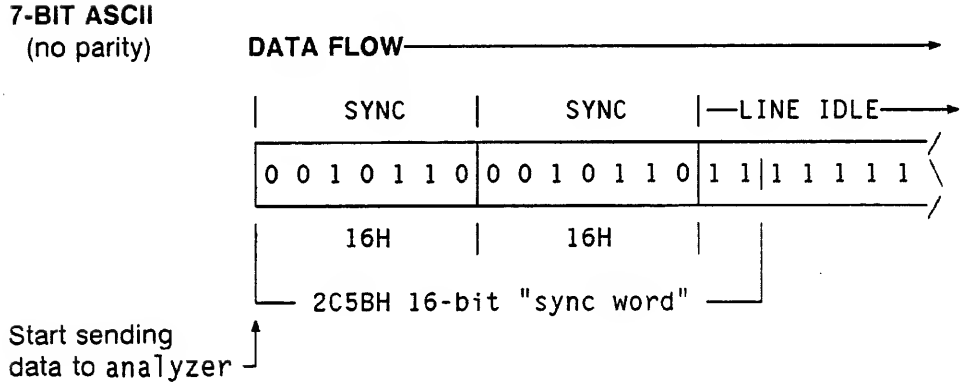


Figure 6-4. 7-Bit ASCII Sync Sequence

In figure 6-5 the sync characters with parity have a longer bit string than the "sync word." The two least significant bits are dropped and the SIO uses 994CH as a comparison to recognize the sync characters.

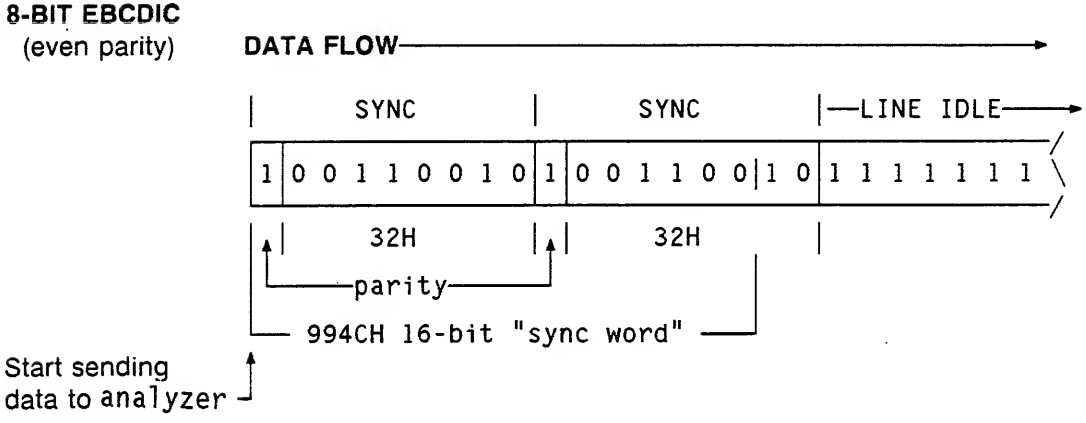


Figure 6-5. 8-Bit EBCDIC Sync Sequence

Block Check Characters

Tha last two characters of the data stream are Block Check Characters (BBC). These characters are actually CRCs and are passed on to the logic analyzer as data. However, they have been altered by the SIO and their value is no longer significant.

Setting Up the HP1650A or HP 16510A for Timing Analysis

The HP 10342B software automatically configures the logic analyzer for state analysis. The logic analyzer can also perform timing analysis on the RS-449 lines. To set up the logic analyzer for timing analysis, you will need to do the following:

1. In the Configuration menu of the logic analyzer, configure Analyzer 2 to be a timing analyzer.

2. Assign pod 3 to Analyzer 2. You should see a display as shown in figure 6-6.

3. Connect probe 3 from the logic analyzer to POD 3 on the HP 10269C.

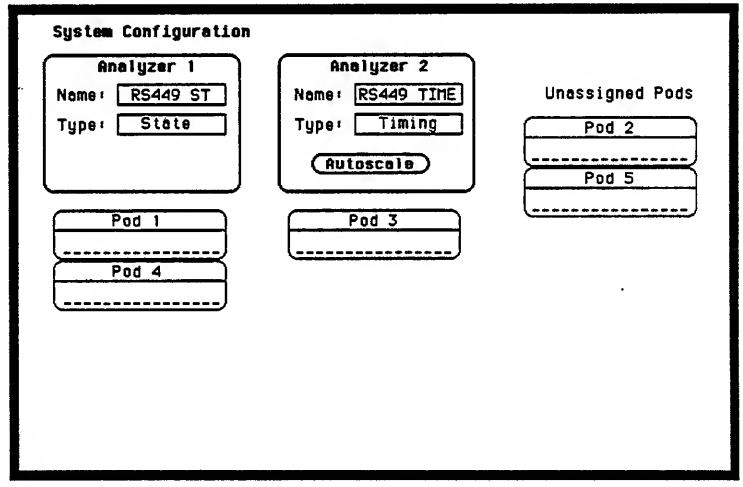


Figure 6-6. Configuration Menu for Timing Analysis with the HP 1650A or HP 16510A

The Format menu will provide a label for each signal.

The following signals are turned off in the Format menu:

RX CLK, TX CLK, RX, TX

To capture these signals with the timing analyzer, turn on the appropriate labels in the Format menu.

Refer to page 6-16 for more information on the timing signals.

Setting Up the HP 1651A for Timing Analysis

The HP 10342B software automatically configures the HP 1651A for state analysis. The logic analyzer can also perform timing analysis on the RS-449 lines. To set up the HP 1651A for timing analysis, you will need to do the following:

1. In the logic analyzer System menu configure Analyzer 2 to be a Timing Analyzer.

2. Assign pod 2 to Analyzer 2. You should see the display as shown in figure 6-7.

3. Move pod 2 from connector 4 to connector 3 on the HP 10269C.

The Format menu of the HP 1651A will provide a label for each signal.

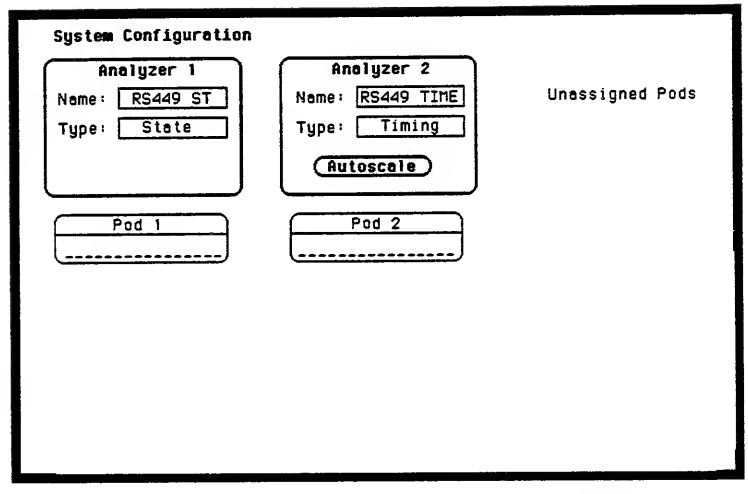


Figure 6-7. Configuration Menu for Timing Analysis with the HP 1651A

Timing Signals

For more information about the timing signals see the "Schematics" section in Chapter 2.

Most timing signals are buffered directly from the RS-449 bus. The TXCLK and RXCLK are clocks selected in the HP 10342B by the DTE/DCE switch and front-panel setup.

On asynchronous buses, the RX CLK and TX CLK are generated by the HP 10342B circuitry and are not signals sent across RS-449.

On synchronous buses, the RX CLK is the REC CLK signal (RT, pins 8 and 26). The TX CLK is either the DTE CLK signal (TT, pins 17 and 35) or the DCE CLK signal (ST, pins 5 and 23), depending on the setting of the DTE/DCE switch on the HP 10342B.

The Receiver Ready (RR) is also buffered directly from the RS-449 bus.

The timing signals supplied to the logic analyzer are of the opposite sense to the mark/space definition in the RS-449 standard (see figure 6-8). The line receivers buffer, invert, and convert the RS-449 signals to TTL.

Though the timing signals are of the opposite sense to that defined by the RS-449 specification, they are of the same sense as the signals supplied to the RS-449 line drivers in the DCE. This makes it easier to compare the output (TTL) of the asynchronous receiver/transmitter in the DCE to the TTL signal applied to the SIO in the DTE.

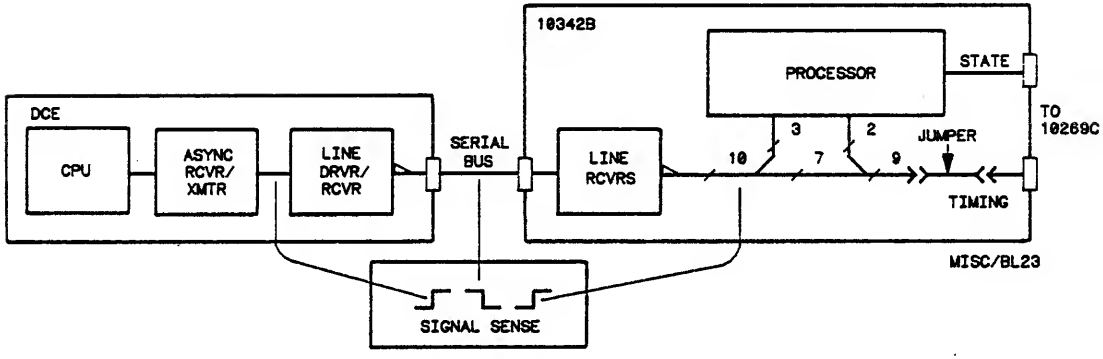


Figure 6-8. Signal Sense Diagram

A HP-IB Overview

Introduction

HP-IB is the Hewlett-Packard implementation of IEEE Standard 488-1978. The following is a brief overview of HP-IB. If additional information is needed obtain the standard from the appropriate source.

The HP-IB

The HP-IB employs a 16-line bus to interconnect up to 15 instruments. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight of the lines are used to transmit data and the remaining eight are used for data transfer control (handshake) and bus management. Data is transferred by means of an interlocked "handshake," permitting asynchronous communication over a wide range of data rates.

The HP-IB structure is diagrammed in figure A-1. Four types of devices may be used on the bus based on their functions:

(1) devices only able to talk;
(2) devices only able to listen;
(3) devices able to talk and listen;
(4) devices able to talk, listen, and control.

The simplest instrument is one that only talks. When signaled this device enters its output on the data bus lines in a fixed configuration. The configuration may be altered only by front-panel control.

Devices that only listen respond to data from the HP-IB data lines. In the case of a signal generator, this data could cause the instrument to output signals of different amplitude and frequency, external to the bus. Printers are frequently listen-only instruments.

A digital multimeter is a device that listens and talks. The multimeter is configured by signals from the controller, takes the requested reading, and returns the results on the bus.

The controller, along with talk and listen capabilities, controls all operations on the interface bus.

As shown in figure A-1, the 16 lines of the HP-IB form three functional groups: five lines for interface management, three lines for handshake (data byte transfer) control, and eight bidirectional lines for carrying data.

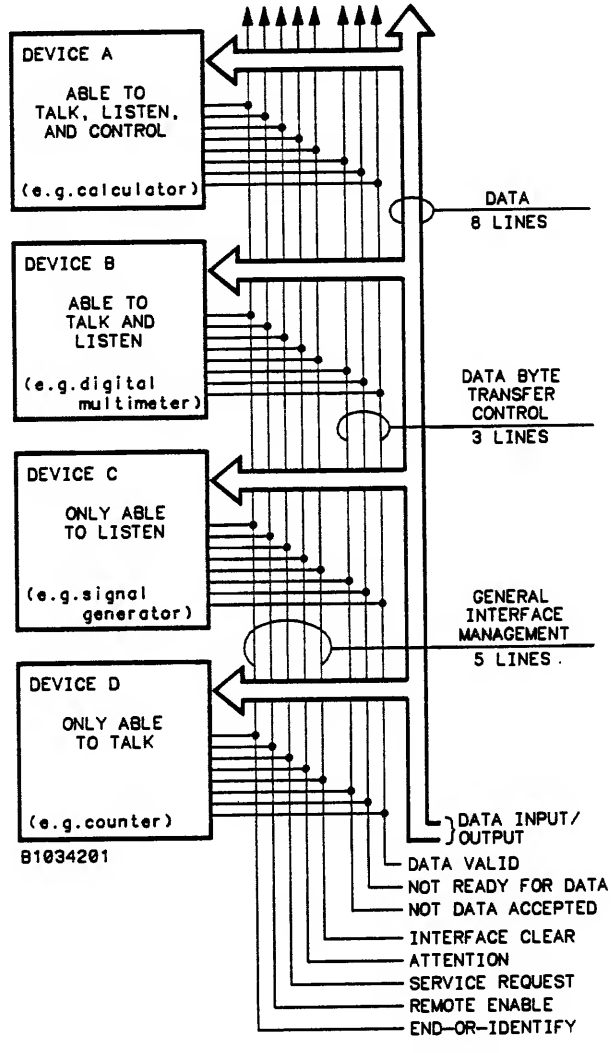


Figure A-1. HP-IB Interface Capabilities and Bus Structure

Interface Management Lines

1. Attention (ATN) specifies how and by which devices data on the data input/output (DIO) lines is to be interpreted. ATN is pulled low for commands (Command Mode) and released for data by the controller.

   In command mode the controller is active and all other devices are waiting for instructions. Command Mode instructions which can be issued by the controller fall into five groups:

   a. Talker Address Group (TAG) commands enable a specific device to talk. Only one device at a time may act as the talker. When the controller addresses one device to talk, the previous talker is automatically unaddressed and ceases to be a talker.

   b. Listener Address Group (LAG) commands enable a specific device to listen. Up to 14 devices at a time may be listeners.

   c. Universal Command Group (UCG) commands cause all bus devices capable of responding to these commands from the controller to do so at any time regardless of whether they are addressed.

   d. Addressed Command Group (ACG) commands are similar to universal commands except that they are recognized only by devices that are addressed as listeners only.

   e. Secondary Command Group (SCG) commands are used when addressing extended listeners and talkers, or enabling the parallel poll.

2. Interface Clear (IFC) puts the entire system into a predefined quiescent state.

3. Service Request (SRQ) is used by a device to indicate a need for attention and to request an interruption of the current sequence of events.

4. Remote Enable (REN), in conjunction with other messages, selects between alternate sources of device programming data (typically HP-IB vs front panel).

5. End or Identify (EOI) indicates the end of a multiple-byte transfer sequence, or, with ATN executes a polling sequence.

The Unlisten Address Command (UNL) unaddresses all listeners that have been previously addressed to listen. The Untalk Address Command (UNT) unaddresses any talker that has been previously addressed to talk.

Handshake Lines

1. Data Valid (DAV) indicates the availability and validity of information on the data lines.

2. Not Ready For Data (NRFD) indicates the state of readiness of devices to accept data.

3. Not Data Accepted (NDAC) indicates the condition of acceptance of data by device(s).

The DAV, NRFD, and NDAC lines operate in a three-wire interlocked handshake process to transfer each data byte across an interface (see figure A-2).

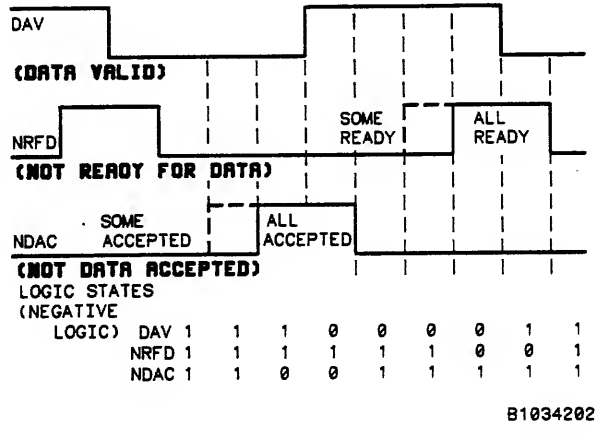


Figure A-2. HP-IB Handshake Sequence

A handshake sequence is entered with the listener-controlled NRFD and NDAC both low. Line DAV is high. As each listener is ready to accept data, it releases its Not Ready For Data (NRFD) line. When all listeners have released their NRFD line, pull-up resistors on the line pull NRFD high. The talker signals new Data Valid by pulling the DAV line low. Listeners respond by pulling their NRFD outputs low. During the period that listeners accept data, they release the Not Data Accepted (NDAC) line. When data has been accepted by all the listeners, the NDAC line goes high. Acknowledgment by the talker releases the DAV line, and the handshake is completed by the listeners by pulling the NDAC low. A legal handshake must proceed in the manner shown in figure A-2. Note that the NRFD and NDAC lines may never go high (logic 0) together.

B Serial Interface Comparisons

introduction

The following tables show comparisons between serial interfaces covered in this document and interfaces not directly covered. Those not directly covered in this document are shown here for reference purposes.

Table B-1. Serial Interface Standards Comparison

Interface Name	Mechanical Standard	Electrical Standard	Functional Standard
RS-232-C	RS-232-C	RS-232-C	RS-232-C
CCITT V.24	ISO-2110	CCITT V.28	CCITT V.24
MIL-188C	RS-232-C	MIL-188C	RS-232-C
RS-449 (balanced)	RS-449	RS-442	RS-449
RS-449 (unbalanced)	RS-449	RS-423	RS-449
CCITT V.35 (balanced)	ISO-2593	CCITT V.11.(X.27)	CCITT V.24
CCITT V.35 (unbalanced)	ISO-2593	CCITT V.10(X.26)	CCITT V.24
MIL-188-114 (balanced)	MIL-188-114	MIL-188-114	MIL-188-114
CCITT X.20 (no clocks)	--	--	--
CCITT X.21 (clocks)	ISO-4903	CCITT V.11	CCITT X.27
CCITT X.21-bis	RS-232-C	CCITT V.10	CCITT X.26

Table B-2. Serial Interface Characteristics Comparison

Interface Type	Interface Connector	Speed	Electrical Maximum	Electrical Threshold
RS-232-C	25 pin	<20Kbps	+25 V	+3 V
RS-449	37 pin	--	--	--
RS-422 (balanced)	--	<10Mbps	+6 V	+0.2 V
RS-423 (unbalanced)	--	<100Kbps	--	--
CCITT V.35	34 pin	56Kbps	(bipolar current)	
CCITT X.20/X.21	15 pin	--	+10 V	+0.3 V
CCITT V.10 (unbalanced)	--	<100Kbps	--	--
CCITT V.11 (balanced)	--	<10Mbps	--	--

Table B-3. Serial Interface Interchange Circuit Comparison

DTE/DCE	EIA RS-232-C	CCITT V.24	EIA RS-449
--	AB Signal Ground	102 Signal Ground	SG Signal Ground
DTE to DCE		102a DTE Common	SC Send Common
DCE to DTE		102b DCE Common	RC Receive Common
DTE to DCE			IS Terminal in Service
DCE to DTE	CE Ring Indicator	125 Calling Indicator	IC Incoming Call
DTE to DCE	CD Data Terminal Ready	108.2 Data Terminal Ready	TR Terminal Read
DCE to DTE	CC Data Set Ready	107 Data Set Ready	DM Data Mode
DTE to DCE	BA Transmitted Data	103 Transmitted Data	SD Send Data
DCE to DTE	BB Received Data	104 Received Data	RD Receive Data

Table B-3. Serial Interface Interchange Circuit Comparison (Continued)

DTE/DCE	EIA RS-232-C	CCITT V.24	EIA RS-449
DTE to DCE	DA Transmitter Signal Element Timing (DTE Source)	113 Transmitter Signal Element Timing (DTE Source)	TT Terminal Timing
DCE to DTE	DB Transmitter Signal Element Timing (DCE Source)	114 Transmitter Signal Element Timing (DCE Source)	ST Send Timing
DCE to DTE	DD Receiver Signal Element Timing	115 Receiver Signal Element Timing (DCE Source)	RT Receive Timing
DTE to DCE	CA Request to Send	105 Request to Send	RS Request to Send
DCE to DTE	CB Clear to Send	106 Ready for Sending	CS Clear to Send
DCE to DTE	CF Received Line Signal Detector	109 Data Channel Received Line Signal Detector	RR Receiver Ready
DCE to DTE	CG Signal Quality Detector	110 Data Signal Quality Detector	SQ Signal Quality
DTE to DCE			NS New Signal
DTE to DCE		126 Select Transmit Frequency	SF Select Frequency
DTE to DCE	CH Data Signal Rate Selector (DTE Source)	111 Data Signaling Rate Selector (DTE Source)	SR Signaling Rate Selector
DCE to DTE	CI Data Signal Rate Selector (DCE Source)	112 Data Signaling Rate Selector (DCE Source)	SI Signaling Rate Indicator

Table B-3. Serial Interface Interchange Circuit Comparison (Continued)

DTE/DCE	EIA RS-232-C	CCITT V.24	EIA RS-449
DTE to DCE DCE to DTE	SBA Secondary Transmitted Data SBB Secondary Received Data	118 Transmitted Backward Channel Data 119 Received Backward Channel Data	SSD Secondary Send Data SRD Secondary Receive Data
DTE to DCE DCE to DTE DCE to DTE	SCA Secondary Request to Send SCB Secondary Clear to Send SCF Secondary Received Line Signal Detector	120 Transmit Backward Channel Line Signal 121 Backward Channel Ready 122 Backward Channel Received Line Signal Detector	SRS Secondary Request to Send SCS Secondary Clear to Send SRR Secondary Receiver Ready
DTE to DCE DTE to DCE DCE to DTE		141 Local Loopback 140 Remote Loopback 142 Test Indicator	LL Local Loopback RL Remote Loopback TM Test Mode
DTE to DCE DCE to DTE		116 Select Standby 117 Standby Indicator	SS Select Standby SB Standby Indicator

C RS-232-C/CCITT V.24 Overview

Introduction

The RS-232-C/CCITT V.24 is a serial interface standard that has predominated for many years. It originated with the requirements for teletype interface, which accounts for the large voltage specifications in the standard. It is still being designed into new equipment though it is being replaced by the RS-449 standard, due to the much higher data speeds of RS-449. The RS-232-C is the EIA standard conforming to the international standard CCITT V.24. It expands on the international standard to include the connector type, pin assignments, and electrical standards.

The following information is intended to cover the main points of RS-232-C. If you need more comprehensive information about the standard, obtain the related documents from the EIA.

The RS-232-C/CCITT V.24

Most voltage interfaces in North America conform to EIA RS-232-C. This standard specifies a 25-pin connector as the standard interface in datacom networks. The connector is shown in figure C-1. The interchange circuitry with pin assignments and CCITT V.24 equivalents is shown in table C-1. In addition to the mechanical and electrical requirements, the standard specifies an operating range of 0 to 20k bps in bit-serial, synchronous, and asynchronous operation.

Mechanical

The signal interface between the Data Communications Equipment (DCE), usually a modem, and the Data Terminal Equipment (DTE), the remote terminal or data processor, is located at the RS-232-C specified connector between two equipments. The female is connected to the DCE and the male to the DTE. Short cables of less than 15 metres (50 feet) are recommended, but longer cables may be used if the load capacitance is suitable. The pin assignments shown in table C-1 must be used, and unassigned pins may carry additional circuits determined by mutual agreement between the communicating parties.

While RS-232-C designates 23 circuits, the number actually used in a given application depends on the requirements of the application. In some modems only nine of the 23 are used.

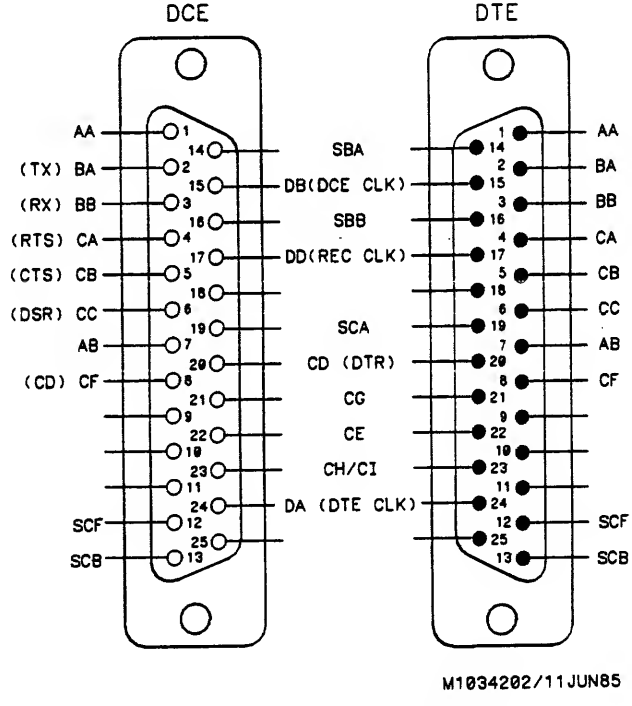


Figure C-1. RS-232-C Connector with Pin Assignments

Table C-1. Interchange Circuits for RS-232-C and CCITT V.24 Equivalents

Pin	Direction DTE/DCE	RS-232-C Circuit	CCITT V.24 Circuit	RS-232-C Description
1	--	AA	101	Protective Ground
2	DTE to DCE	BA	103	Transmitted Data
3	DCE to DTE	BB	104	Received Data
4	DTE to DCE	CA	105	Request to Send
5	DCE to DTE	CB	106	Clear to Send
6	DCE to DTE	CC	107	Data Set Ready
7	--	AB	102	Signal Ground (Common Return)
8	DCE to DTE	CF	109	Received Line Signal Detector
9	--	--	--	(Reserved for Data Set Testing)
10	--	--	--	(Reserved for Data Set Testing)
11	--	--	--	Unassigned
12	DCE to DTE	SCF	122	Secondary Received Line Signal Detector
13	DCE to DTE	SCB	121	Secondary Clear to Send
14	DTE to DCE	SBA	118	Secondary Transmitted Data
15	DCE to DTE	DB	114	Transmitter Signal Element Timing (DCE Source)
16	DCE to DTE	SBB	119	Secondary Received Data
17	DCE to DTE	DD	115	Receiver Signal Element Timing (DCE Source)
18	--	--	--	Unassigned
19	DTE to DCE	SCA	120	Secondary Request to Send
20	DTE to DCE	CD	108.2	Data Terminal Ready
21	DCE to DTE	CG	110	Signal Quality Detector
22	DCE to DTE	CE	125	Ring Indicator
23	DTE to DCE	CH/CI	111/112	Data Signal Rate Detector (DTE/DCE Source)
24	DTE to DCE	DA	113	Transmitter Signal Element Timing (DTE Source)
25	--	--	--	Unassigned

Electrical

Except for protective and signal grounds, all circuits carry bi-polar low-voltage signals that are suitable for electronic circuits. All voltages are measured at the connector with respect to Signal Ground (AB) and cannot exceed ±25 V. The electrical specifications are shown in table C-2.

Control circuits can be designated as fail safe. This means that when power is lost at the transmitter the receiver interprets the signal condition as off.

Table C-2. Condensed Electrical Specifications for EIA RS-232-C

Driver output levels with 3 kohm to 7 kohm load	15 V > V_{OH} > 5 V -5 V > V_{OL}
Driver output voltage with open circuit	|Vo| < 25 V
Driver output impedance with power off	Ro > 300 ohms
Output short circuit current	|Io| < 0.5 A
Driver slew rate	dv/dt < 30 V/μs
Receiver input impedance	7 kohm > Rin > 3 kohm
Receiver input voltage	+15 V compatible with driver
Receiver output with open circuit input	MARK
Receiver output with +3 V input	SPACE
Receiver output with -3 V input	MARK
LOGIC -0- = SPACE = CONTROL ON	+5 V to +15 V
Noise Margin	+3 V to +5 V
Transition Region	-3 V to +3 V
Noise Margin	-3 V to -5 V
LOGIC -1- = MARK = CONTROL OFF	-5 V to -15 V

D RS-449 AND RS-422 Overview

Introduction

In 1975 uniform standards were established governing the electrical parameters and interface between both high-speed and low-speed data communications. These standards, RS-422 and RS-423 respectively, specify characteristics without defining the mechanical interface. RS-422 establishes characteristics of balanced voltage interface circuits, while RS-423 establishes characteristics for unbalanced circuits.

The standard for defining the mechanical and functional characteristics of the RS-422 and RS-423 standards is RS-449. This standard was released in 1977. Only the RS-422 standard will be explained in this appendix.

The RS-449/RS-422

The main differences between the RS-449 standard and the RS-232-C standard are the following:

1. Two connectors, a 37-pin and a 9-pin, replace the 25-pin connector used in RS-232-C applications. The 37-pin connector accommodates the normal interchange circuits while the 9-pin connector is used for secondary channel circuits. Both connectors are from the same family as the RS-232-C connector.

2. Depending on the signaling rate, the cable distance between equipments has been extended to 60 metres (200 feet) from the RS-232-C distance of 15 metres (50 feet).

3. Ten interchange circuits not previously included in RS-232-C have been defined in RS-449.

4. The electrical characteristics (RS-422 and RS-423) in the interface have been completely re-defined. Both balanced and unbalanced circuits may be used within one interface connection. Two categories of circuits are defined: Category I circuits, which may be balanced or unbalanced depending on data rate, and Category II circuits, which are always unbalanced.

With a few additional provisions, equipment conforming to this standard can be used with equipment conforming to RS-232-C standards.

Mechanical and Functional

The basic functional characteristic of the standard (RS-449) is to operate up to a nominal limit of 2M bps in synchronous or non-synchronous communication. The connector is shown in figure D-1 on the next page. Table D-1 shows the interchange circuits with pins, circuit names and mnemonics.

Electrical

The balanced electrical standard (RS-422) for the new interface is too involved to explain here without explaining virtually the entire standard. This is because the higher data rates used with these standards requires more involved specifications. The primary points are:

1. The signal voltage levels are less than |6V| open circuit and less than |3V| at nominal load.

2. The receiver requires a maximum differential voltage of 200 mV to ensure the intended state over the common mode voltage range of -7 V to +7 V. The receiver should operate with a maximum differential input of 12 V.

3. The nominal impedance is 100 ohms and the minimum load impedance is not less than 90 ohms.

4. The input impedance of the receivers should be greater than 4 kohms.

5. The short circuit current is 150 mA.

6. The risetime of the data pulses is less than 0.1(bit period) when the bit period is greater than 200 ns and less than 20 ns when the bit period is less than 200 ns.

The unbalanced electrical standard (RS-423) is also too involved to explain in this document and is only mentioned because many of the lines (Category II) are operated unbalanced at all times. The characteristics for the unbalanced signals are much the same as for the balanced signals once the lack of the differential characteristic is taken into account. Consult the EIA Standard for further information.

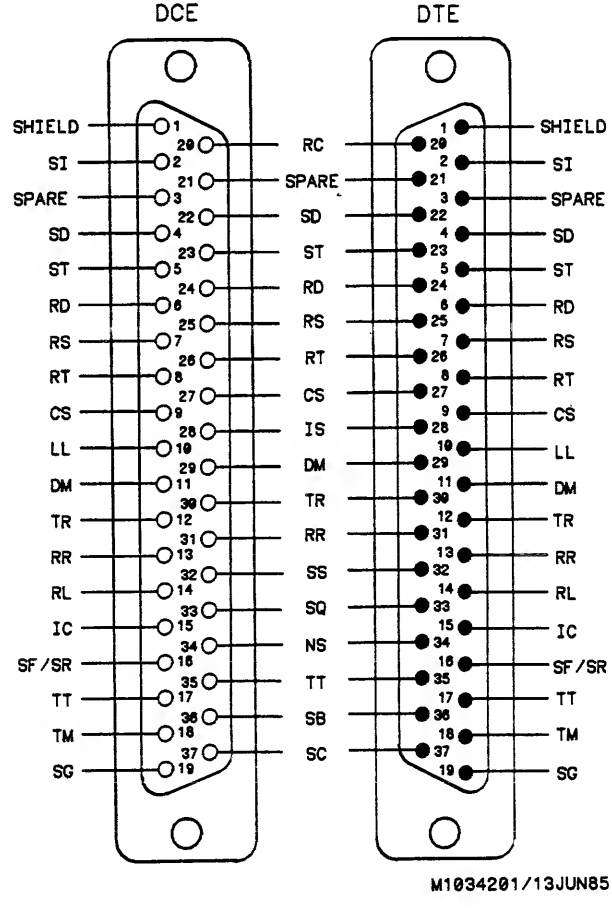


Figure D-1. RS-449 Connector with Pin Assignments

Table D-1. Interchange Circuits for RS-449

Pins	Direction DTE/DCE	Circuit	Category	Description
1	--	SHIELD	--	--
2	DCE to DTE	SI	II	Signaling Rate Indicator
20	DCE to DTE	RC	II	Receive Common
3	--	SPARE	--	--
21	--	SPARE	--	--
4 22	DTE to DCE	SD	I	Send Data
5 23	DCE to DTE	ST	I	Send Timing
6 24	DCE to DTE	RD	I	Receive Data
7 25	DTE to DCE	RS	I	Request to Send
8 26	DCE to DTE	RT	I	Receive Timing
9 27	DCE to DTE	CS	I	Clear to Send
10	DTE to DCE	LL	II	Local Loopback
28	DTE to DCE	IS	II	Terminal in Service
11 29	DCE to DTE	DM	I	Data Mode
12 30	DTE to DCE	TR	I	Terminal Ready
13 31	DCE to DTE	RR	I	Receiver Ready
14	DTE to DCE	RL	II	Remote Loopback
32	DTE to DCE	SS	II	Select Standby
15	DCE to DTE	IC	II	Incoming Call
33	DCE to DTE	SQ	II	Signal Quality
16	DTE to DCE	SF/SR	II	Select Frequency/ Signaling Rate Selector
34	DTE to DCE	NS	II	New Signal
17 35	DTE to DCE	TT	I	Terminal Timing
18	DCE to DTE	TM	II	Test Mode
36	DCE to DTE	SB	II	Standby Indicator
19	DTE to DCE	SG	II	Signal Ground
37	DTE to DCE	SC	II	Send Common

E Using the HP 10342B with other CPU Interfaces

The HP 1650A and HP 16510A logic analyzers can be configured as two state analyzers. This configuration can be used to monitor a microprocessor and a bus simultaneously. This allows you to analyze the interaction between a microprocessor and a port.

To do this you must have an HP 10342B Bus Preprocessor, two HP 10269C General Purpose probe Interfaces, and a preprocessor for the microprocessor that you're using.

The following example will show you how to configure your logic analyzer to monitor an RS-232C port and a microprocessor simultaneously. Although the example uses a 68000 microprocessor, this technique will work with any microprocessor that can be analyzed with three logic analyze probes or less.

1. Set all the switches on the 68000 Preprocessor (HP 10311B) to the correct position and install the HP 10311B in the HP 10269C General Purpose Probe Interface.

2. Connect the 68000 Preprocessor cables to the target system.

3. Install the RS-232C Preprocessor (HP 10342B) in the second HP 10269C General Purpose Probe Interface.

4. Connect the RS-232C Preprocessor cables to the RS-232C port and set the front-panel switches on the HP 10342B to match the setup of the port.

5. Plug the logic analyzer probes into the HP 10269C as follows:

HP 1650A and 16510A Pod	(into)	HP 10269C Connector
		HP 10269C-1*
1		1
2		2
3		3
		HP 10269C-2**
4		1
5		4

* HP 10269C-1 represents the HP 10269C with the 68000 Preprocessor.

** HP 10269C-2 represents the HP 10269C with the RS-232C Preprocessor.

6. Load the 68000 configuration and inverse assembler from the disc provided with the 68000 Preprocessor.

7. Bring up the logic analyzer System menu and perform the following:

   a. Configure Analyzer 2 of the logic analyzer to be a state analyzer.

   b. Assign pods 4 and 5 to Analyzer 2 of the logic analyzer.

8. Bring up the Format menu of Analyzer 2 and set up the labels and configuration for pods 4 and 5 as shown in figure E-1.

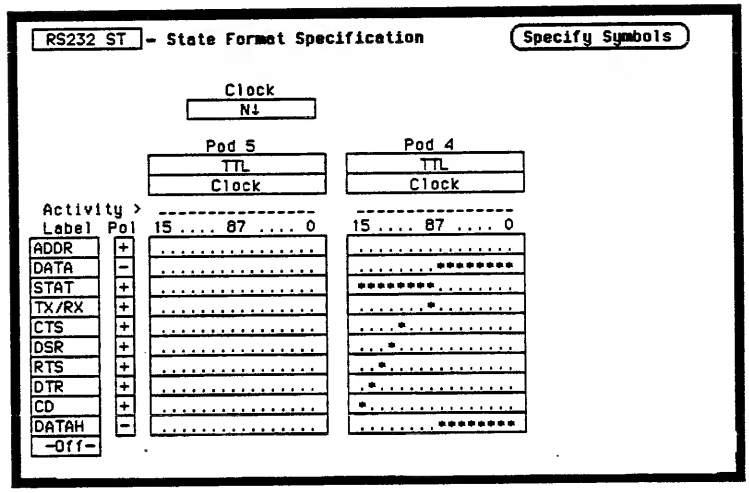


Figure E-1. Format menu for Analyzer 2

9. Assign the following edge of the N clock to pods 4 and 5 as shown in figure E-1.

10. Load IRS232_I (inverse assembler file) into Analyzer 2 of the logic analyzer.

11. Go to the Display menu for Analyzer 2 and change the base of the data label from hexadecimal (HEX) to "Invasm."

12. This configuration allows you to view the microprocessor's and the port's activity individually, or simultaneously using a "mixed-mode" display. Select the display that is most useful for your application.

13. When you have finished configuring the logic analyzer, bring up the Disc menu of the logic analyzer and store this configuration in a separate file for later use. If both the 68000 inverse assembler and the RS-232C inverse assembler are on the same disc as this configuration file, the inverse assemblers will be automatically loaded when the configuration is loaded.

10342-90912

PRINTED IN U.S.A.